Introduction to Robotics

ISS3180-01

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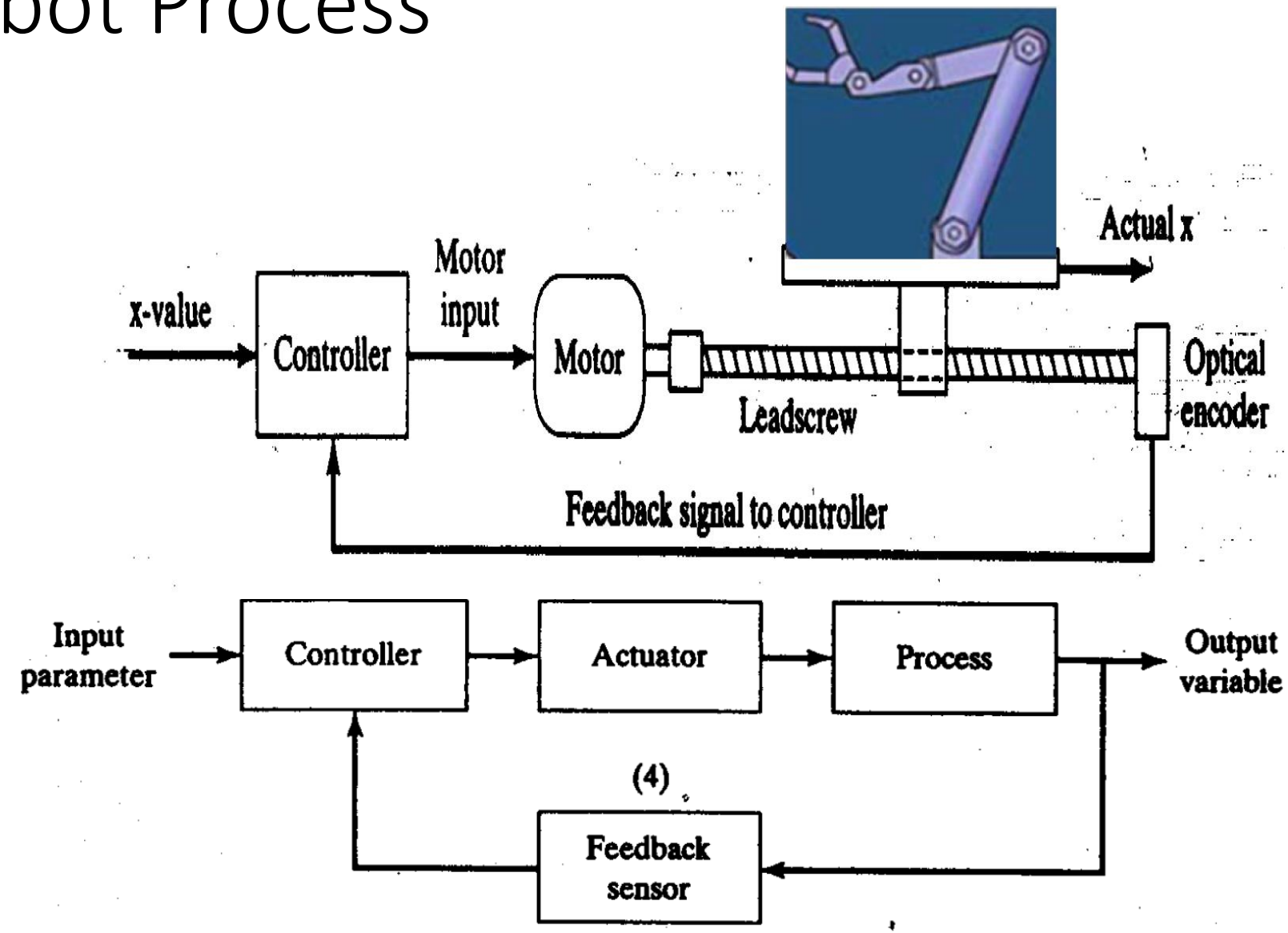
Robot Process



Robot Control Unit and Feedback

- Controller
  - 8051 Microcontroller
  - Programmable Logic Controllers
- Signal Converters
  - Analog to Digital
  - Digital to Analog

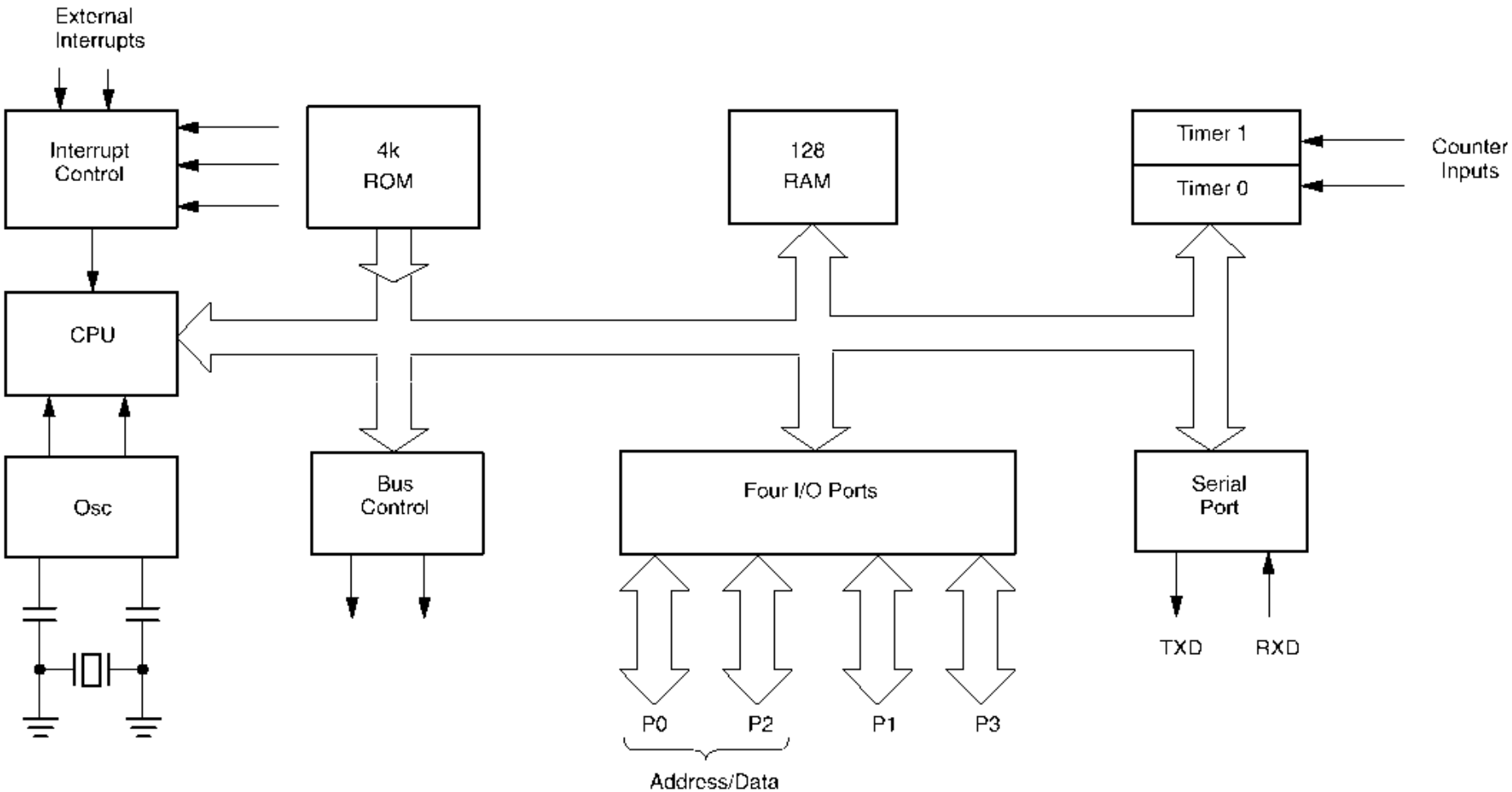
Functions of Controllers

- on-off control
- sequential control
- feedback control
- motion control

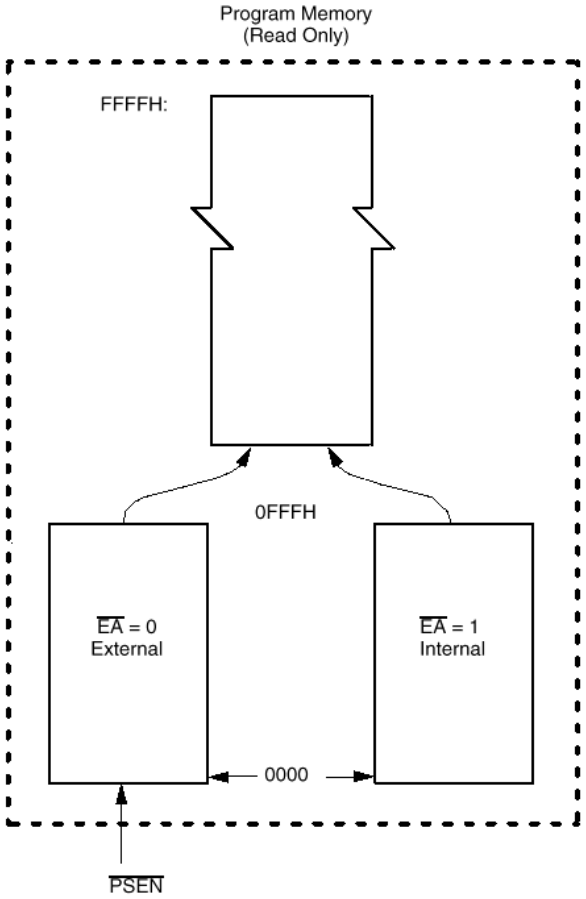
What to Control?

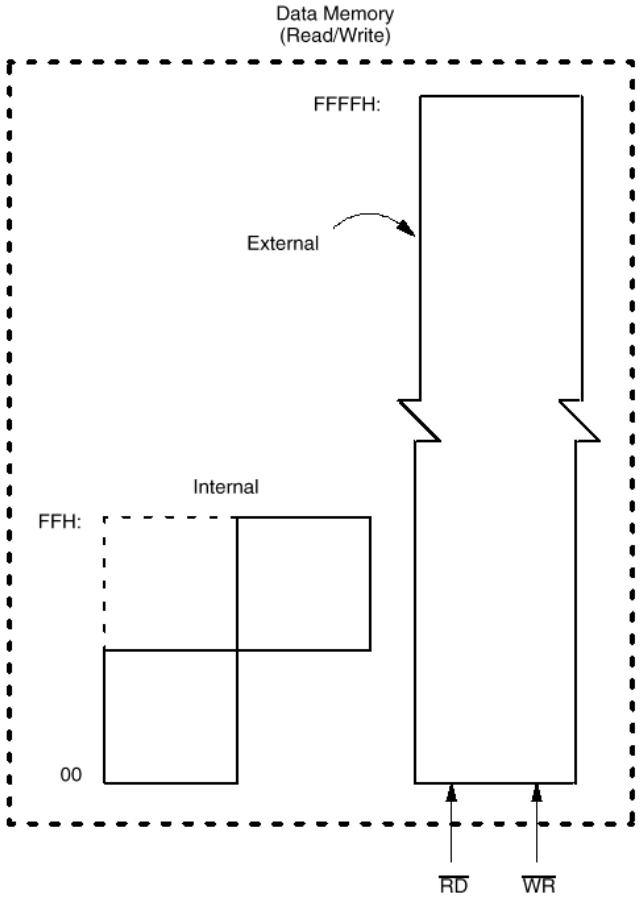
- mechanical control
  - cam, governor, etc.
- pneumatic control
  - compressed air, valves, etc.
- electromechanical control
  - switches, relays, a timer, counters, etc.
- electronics control
  - similar to electromechanical control, except uses electronic switches
- computer control
  - computational, algorithm, etc.

80C51 Block Diagram



80C51 Memory





8051 Memory

- The data width is 8 bits
- Registers are 8 bits
- Addresses are 8 bits
  - i.e. addresses for only 256 bytes!
  - PC is 16 bits (up to 64K program memory)
  - DPTR is 16 bits (for external data - up to 64K)
- C types
  - char - 8 bits <-- use this if at all possible!
  - short - 16 bits
  - int - 16 bits
  - long - 32 bits
  - float - 32 bits
- C standard **`signed/unsigned`**

Accessing External Memory

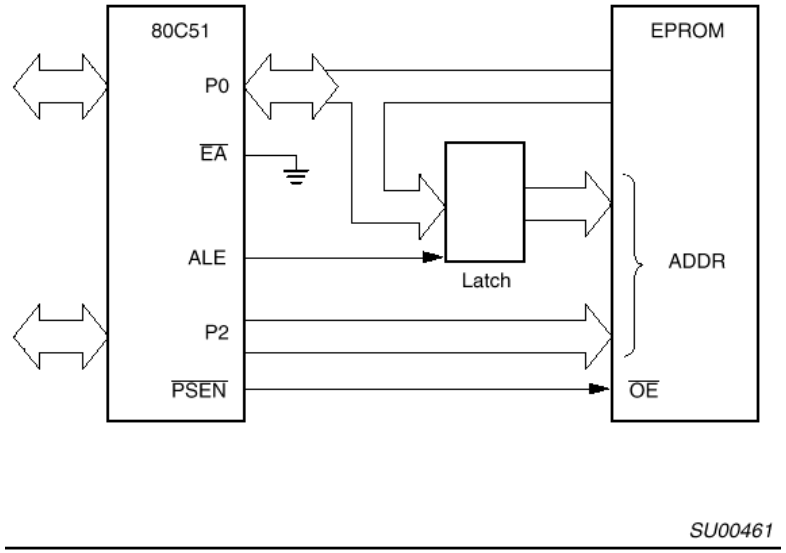


Figure 4. Executing from External Program Memory

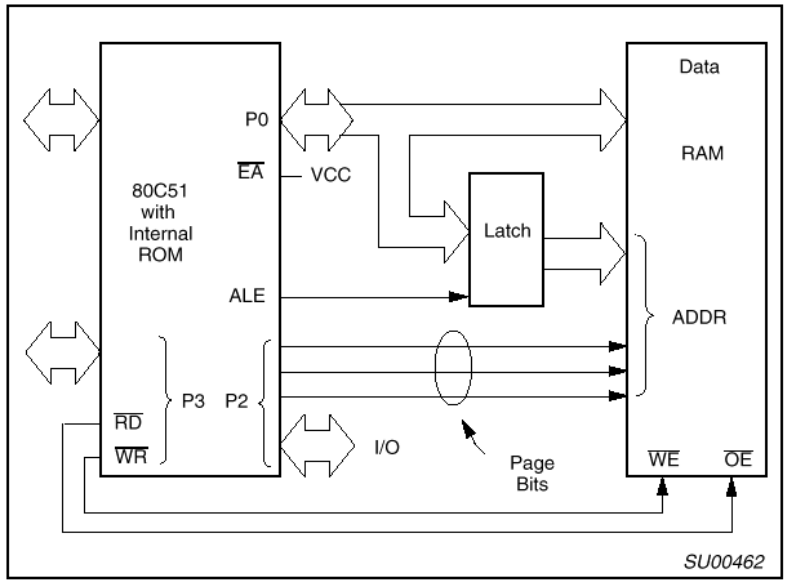
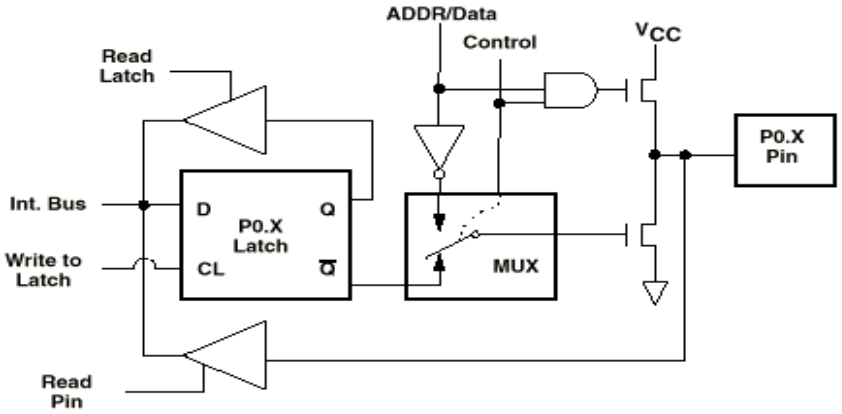


Figure 5. Accessing External Data Memory

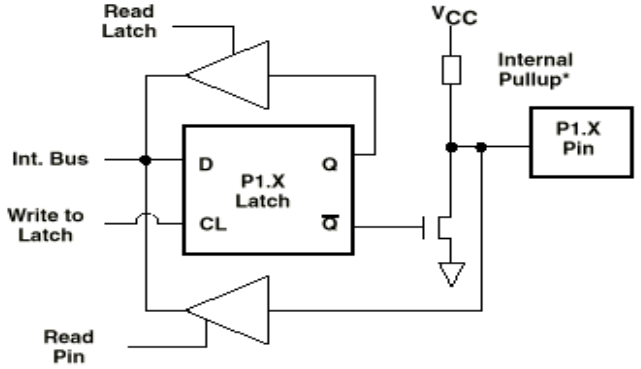
Ports

- Port 0 - external memory access
  - low address byte/data
- Port 2 - external memory access
  - high address byte
- Port 1 - general purpose I/O
  - pins 0, 1 for timer/counter 2
- Port 3 - Special features
  - 0 - RxD: serial input
  - 1 - TxD: serial output
  - 2 - INT0: external interrupt
  - 3 - INT1: external interrupt
  - 4 - T0: timer/counter 0 external input
  - 5 - T1: timer/counter 1 external input
  - 6 - WR: external data memory write strobe
  - 7 - RD: external data memory read strobe

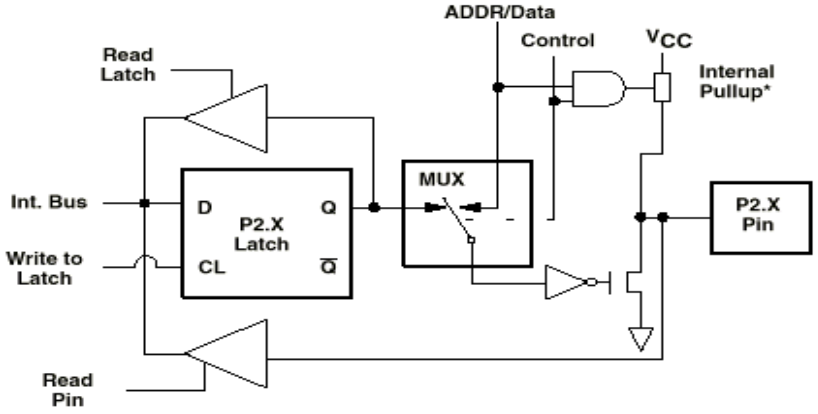
Ports



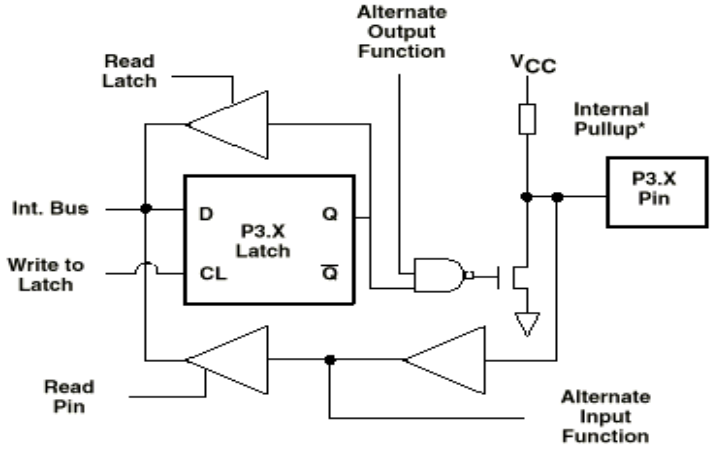
a. Port 0 Bit



b. Port 1 Bit



c. Port 2 Bit



d. Port 3 Bit

Ports

- Port 0 - true bi-directional
- Port 1-3 - have internal pullups that will source current
- Output pins:
  - Just write 0/1 to the bit/byte
- Input pins:
  - Output latch must have a 1 (reset state)
    - Turns off the pulldown
    - pullup must be pulled down by external driver
  - Just read the bit/byte

Program Status Word

- Register set select
- Status bits

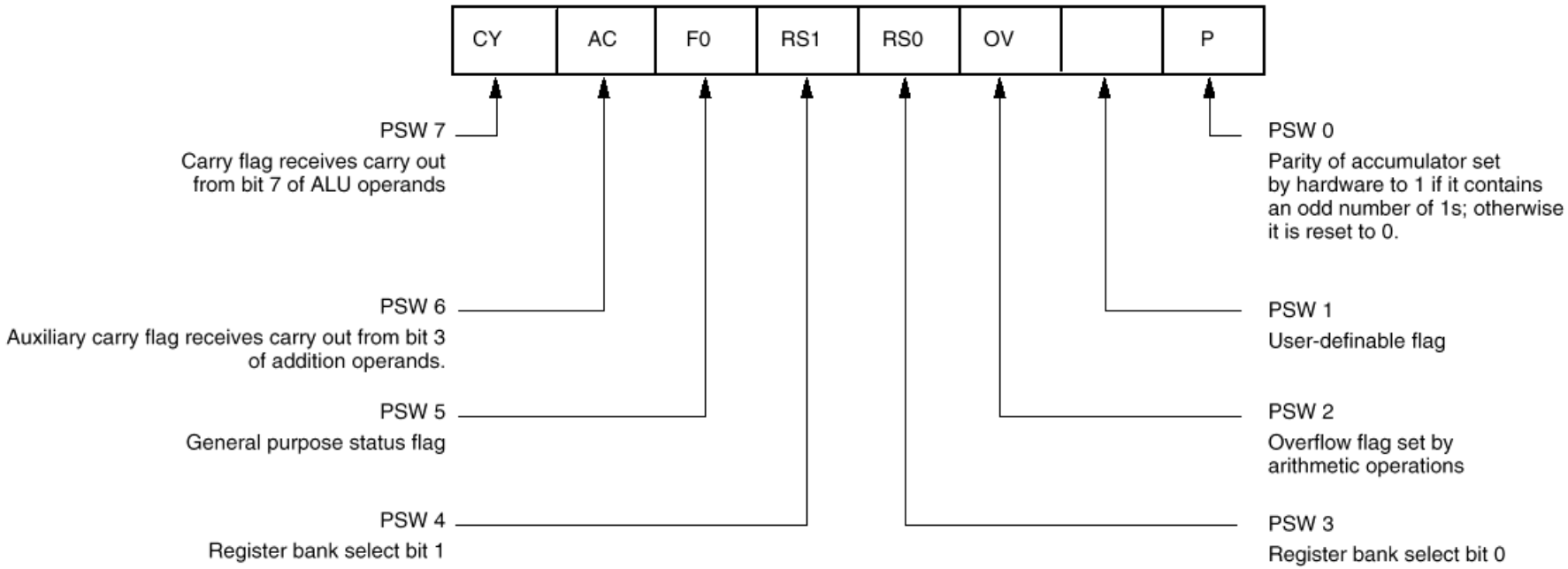


Figure 10. PSW (Program Status Word) Register in 80C51 Devices

Instruction Timing

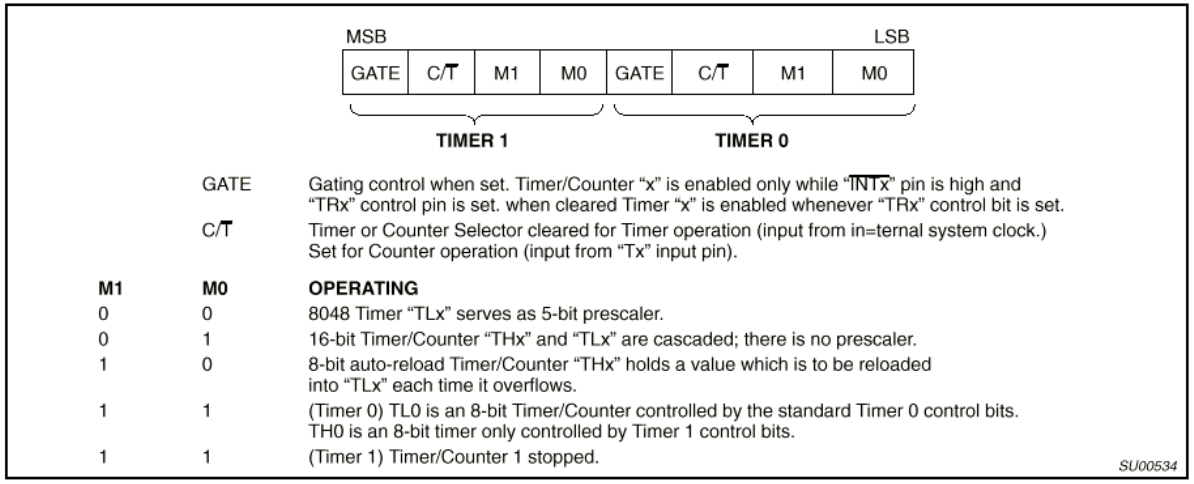
- One “machine cycle” = 6 states (S1 - S6)
- One state = 2 clock cycles
  - One “machine cycle” = 12 clock cycles
- Instructions take 1 - 4 cycles
  - e.g. 1 cycle instructions: ADD, MOV, SETB, NOP
  - e.g. 2 cycle instructions: JMP, JZ
  - 4 cycle instructions: MUL, DIV

Timers

- Base 8051 has 2 timers
  - we have 3 in the Atmel 89C55
- Timer mode
  - Increments every machine cycle (12 clock cycles)
- Counter mode
  - Increments when T0/T1 go from 1 - 0 (external signal)
- Access timer value directly
- Timer can cause an interrupt
- Timer 1 can be used to provide programmable baud rate for serial communications
- Timer/Counter operation
  - Mode control register (TMOD)
  - Control register (TCON)

Mode Control Register (TMOD)

- Modes 0-3
- GATE - allows external pin to enable timer (e.g. external pulse)
  - 0: INT pin not used
  - 1: counter enabled by INT pin (port 3.2, 3.3)
- C/T - indicates timer or counter mode



MSB							LSB
GATE	C/$\overline{T}$	M1	M0	GATE	C/$\overline{T}$	M1	M0
TIMER 1				TIMER 0			

	GATE	Gating control when set. Timer/Counter "x" is enabled only while "$\overline{INTx}$" pin is high and "TRx" control pin is set. when cleared Timer "x" is enabled whenever "TRx" control bit is set.
	C/$\overline{T}$	Timer or Counter Selector cleared for Timer operation (input from in=ternal system clock.) Set for Counter operation (input from "Tx" input pin).
M1	**M0**	**OPERATING**
0	0	8048 Timer "TLx" serves as 5-bit prescaler.
0	1	16-bit Timer/Counter "THx" and "TLx" are cascaded; there is no prescaler.
1	0	8-bit auto-reload Timer/Counter "THx" holds a value which is to be reloaded into "TLx" each time it overflows.
1	1	(Timer 0) TL0 is an 8-bit Timer/Counter controlled by the standard Timer 0 control bits. TH0 is an 8-bit timer only controlled by Timer 1 control bits.
1	1	(Timer 1) Timer/Counter 1 stopped.

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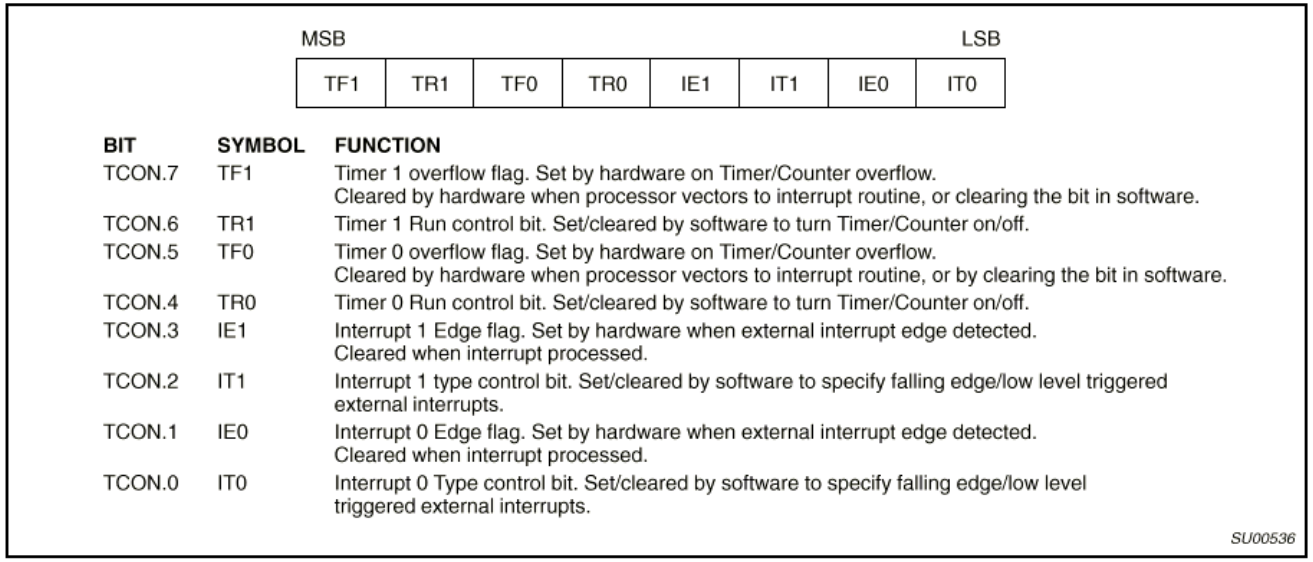
Figure 6. Timer/Counter Mode Control (TMOD) Register

Timer/Counter Control Register (TCON)

- TR - enable timer/counter
- TF - overflow flag: can cause interrupt
- IE/IT - external interrupts and type control
  - not related to the timer/counter



MSB							LSB
TF1	TR1	TF0	TR0	IE1	IT1	IE0	IT0

BIT	SYMBOL	FUNCTION
TCON.7	TF1	Timer 1 overflow flag. Set by hardware on Timer/Counter overflow. Cleared by hardware when processor vectors to interrupt routine, or clearing the bit in software.
TCON.6	TR1	Timer 1 Run control bit. Set/cleared by software to turn Timer/Counter on/off.
TCON.5	TF0	Timer 0 overflow flag. Set by hardware on Timer/Counter overflow. Cleared by hardware when processor vectors to interrupt routine, or by clearing the bit in software.
TCON.4	TR0	Timer 0 Run control bit. Set/cleared by software to turn Timer/Counter on/off.
TCON.3	IE1	Interrupt 1 Edge flag. Set by hardware when external interrupt edge detected. Cleared when interrupt processed.
TCON.2	IT1	Interrupt 1 type control bit. Set/cleared by software to specify falling edge/low level triggered external interrupts.
TCON.1	IE0	Interrupt 0 Edge flag. Set by hardware when external interrupt edge detected. Cleared when interrupt processed.
TCON.0	IT0	Interrupt 0 Type control bit. Set/cleared by software to specify falling edge/low level triggered external interrupts.

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Figure 8. Timer/Counter Control (TCON) Register

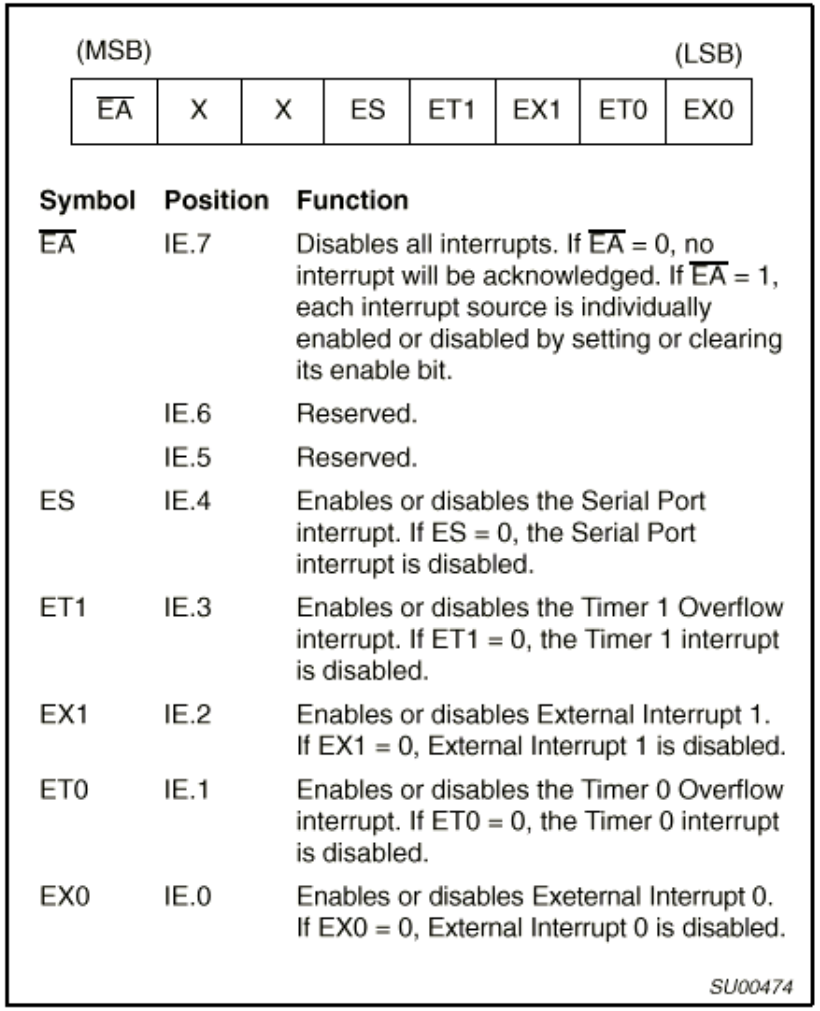
Interrupts

- Allow parallel tasking
  - Interrupt routine runs in “background”
- Allow fast, low-overhead interaction with environment
  - Don’t have to poll
  - Immediate reaction
- An automatic function call
  - Easy to program
- 8051 Interrupts
  - Serial port - wake up when data arrives/data has left
  - Timer 0 overflow
  - Timer 1 overflow
  - External interrupt 0
  - External interrupt 1

Timer Interrupts

- Wakeup after N clock cycles, i.e. at a specified time
- Wakeup every N clock cycles (auto reload)
  - Allows simple task scheduling
  - Clients queue function calls for time i
  - Interrupt routine calls functions at the right time
- Wakeup after N events have occurred on an input

Controlling Interrupts: Enables and Priority



(MSB) (LSB)

$\overline{EA}$	X	X	ES	ET1	EX1	ET0	EX0

Symbol	Position	Function
$\overline{EA}$	IE.7	Disables all interrupts. If $\overline{EA}$ = 0, no interrupt will be acknowledged. If $\overline{EA}$ = 1, each interrupt source is individually enabled or disabled by setting or clearing its enable bit.
	IE.6	Reserved.
	IE.5	Reserved.
ES	IE.4	Enables or disables the Serial Port interrupt. If ES = 0, the Serial Port interrupt is disabled.
ET1	IE.3	Enables or disables the Timer 1 Overflow interrupt. If ET1 = 0, the Timer 1 interrupt is disabled.
EX1	IE.2	Enables or disables External Interrupt 1. If EX1 = 0, External Interrupt 1 is disabled.
ET0	IE.1	Enables or disables the Timer 0 Overflow interrupt. If ET0 = 0, the Timer 0 interrupt is disabled.
EX0	IE.0	Enables or disables Exeternal Interrupt 0. If EX0 = 0, External Interrupt 0 is disabled.

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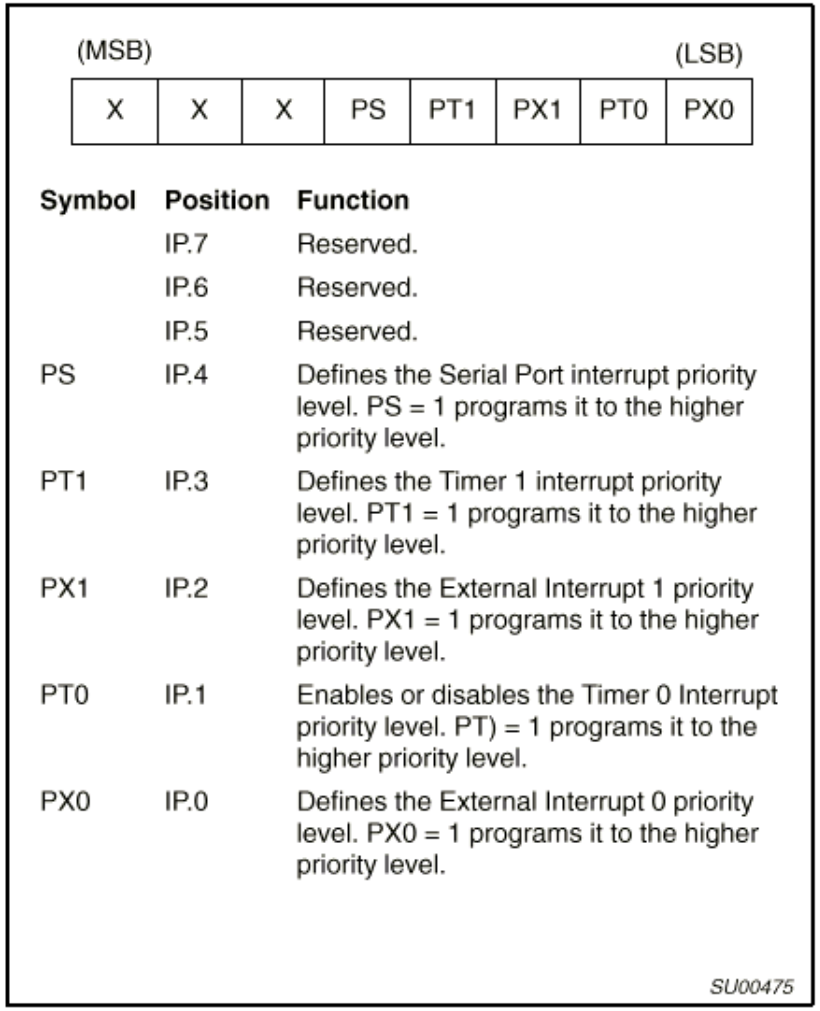
Figure 17. Interrupt Enable (IE) Register



(MSB) (LSB)

X	X	X	PS	PT1	PX1	PT0	PX0

Symbol	Position	Function
	IP.7	Reserved.
	IP.6	Reserved.
	IP.5	Reserved.
PS	IP.4	Defines the Serial Port interrupt priority level. PS = 1 programs it to the higher priority level.
PT1	IP.3	Defines the Timer 1 interrupt priority level. PT1 = 1 programs it to the higher priority level.
PX1	IP.2	Defines the External Interrupt 1 priority level. PX1 = 1 programs it to the higher priority level.
PT0	IP.1	Enables or disables the Timer 0 Interrupt priority level. PT) = 1 programs it to the higher priority level.
PX0	IP.0	Defines the External Interrupt 0 priority level. PX0 = 1 programs it to the higher priority level.

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Figure 18. Interrupt Priority (IP) Register

Interrupt Priorities

- Two levels of priority
  - Set an interrupt priority using the interrupt priority register
  - A high-priority interrupt can interrupt an low-priority interrupt routine
  - In no other case is an interrupt allowed
  - An interrupt routine can always disable interrupts explicitly
    - But you don’t want to do this
- Priority chain within priority levels
  - Choose a winner if two interrupts happen simultaneously
  - Order shown on previous page

External Interrupts

- Can interrupt using the INT0 or INT1 pins (port 3: pin 2,3)
  - Interrupt on level or falling edge of signal (TCON specifies which)
  - Pin is sampled once every 12 clock cycles
    - for interrupt on edge, signal must be high 12 cycles, low 12 cycles
  - Response time takes at least 3 instuctions cycles
    - 1 to sample
    - 2 for call to interrupt routine
    - more if a long instruction is in progress (up to 6 more)

PLCs

- Review brief history of PLCs and manufacturing control systems
- Introduce the concepts of discrete control of manufacturing
- Overview ladder logic programming

Readings

- Chapter 10 of ***Computer Aided Manufacturing***, Chang, Chang, T.C. and Wysk, R. A. and Wang, H.P., 3rd Edition, 2006.

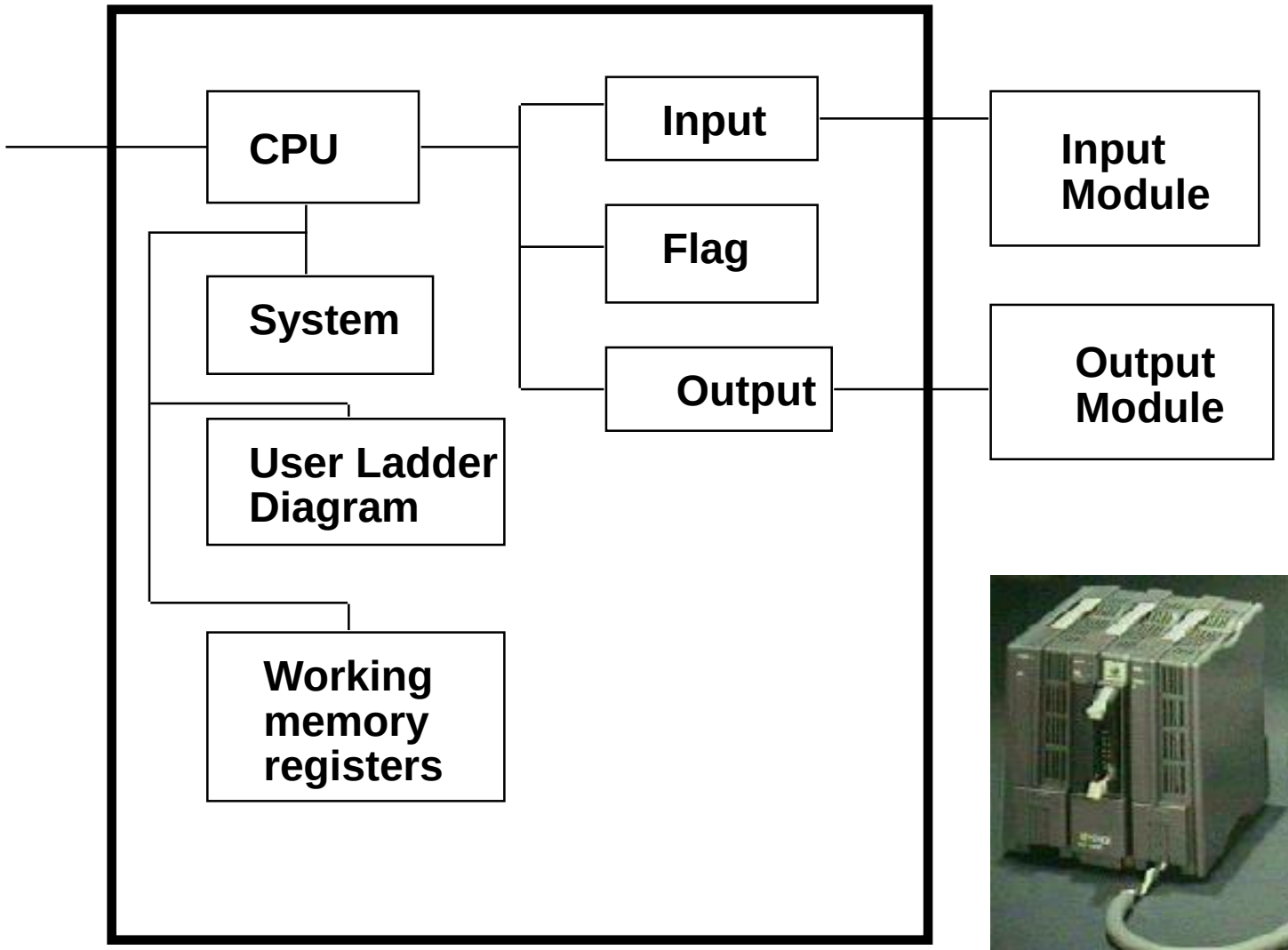
Types of control

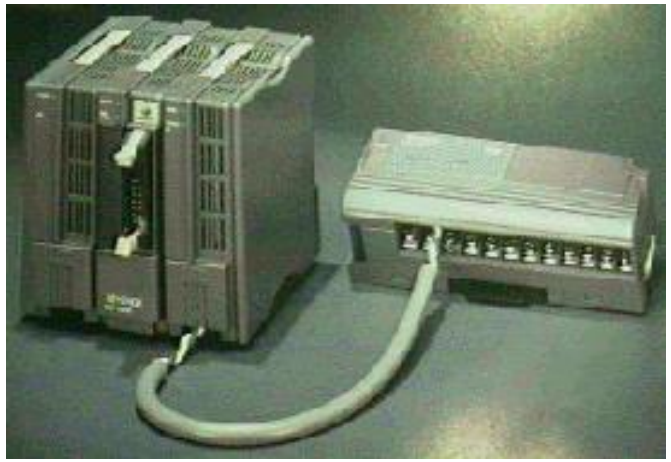
- Temporal – control based in time
- State – control based in state level
- Hybrid – both temporal and state

PURPOSE OF Programmable Logic Controllers (PLCs)

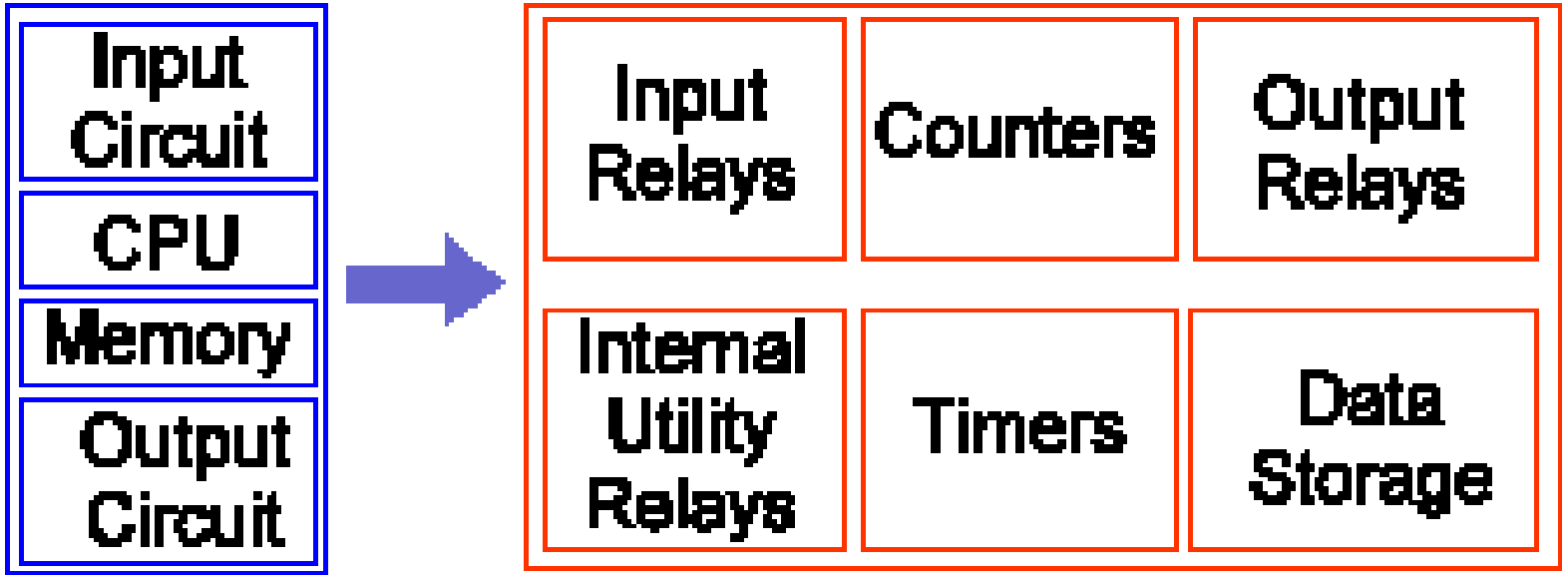
- Initially designed to replace relay logic boards
  - Sequence device actuation
  - Coordinate activities
- Accepts input from a series of switches
- Sends output to devices or relays

PLC


CPU
System
User Ladder Diagram
Working memory registers
Input
Flag
Output
Input Module
Output Module



PLC Configuration



What devices does a PLC interact with?

- **INPUT RELAYS-**(contacts)These are connected to the outside world. They physically exist and receive signals from switches, sensors, etc. Typically they are not relays but rather they are transistors.
- **INTERNAL UTILITY RELAYS-**(contacts) These do not receive signals from the outside world nor do they physically exist. They are simulated relays and are what enables a PLC to eliminate external relays. There are also some special relays that are dedicated to performing only one task. Some are always on while some are always off. Some are on only once during power-on and are typically used for initializing data that was stored.
- **COUNTER**S-These again do not physically exist. They are simulated counters and they can be programmed to count pulses. Typically these counters can count up, down or both up and down. Since they are simulated they are limited in their counting speed. Some manufacturers also include high-speed counters that are hardware based. We can think of these as physically existing. Most times these counters can count up, down or up and down.

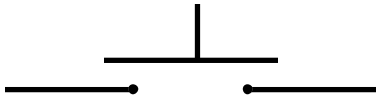
What devices does a PLC interact with? Continued

- **TIMERS**-These also do not physically exist. They come in many varieties and increments. The most common type is an on-delay type. Others include off-delay and both retentive and non-retentive types. Increments vary from 1ms through 1s.
- **OUTPUT RELAYS**-(coils)These are connected to the outside world. They physically exist and send on/off signals to solenoids, lights, etc. They can be transistors, relays, or triacs depending upon the model chosen.
- **DATA STORAGE**-Typically there are registers assigned to simply store data. They are usually used as temporary storage for math or data manipulation. They can also typically be used to store data when power is removed from the PLC. Upon power-up they will still have the same contents as before power was removed. Very convenient and necessary!!

SWITCHES

Non-locking

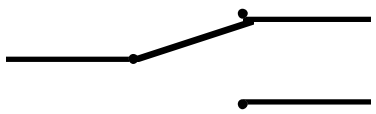
Locking



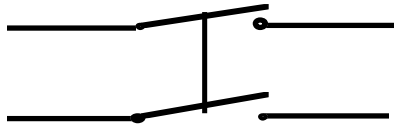
Normally Open

Normally Closed

SPDT

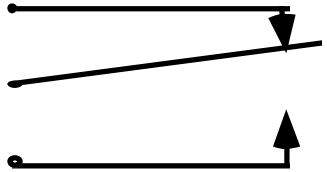


Multiple Throw

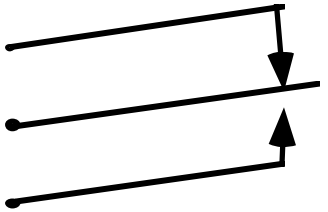


Multiple Pole

DPST



Break-before-make

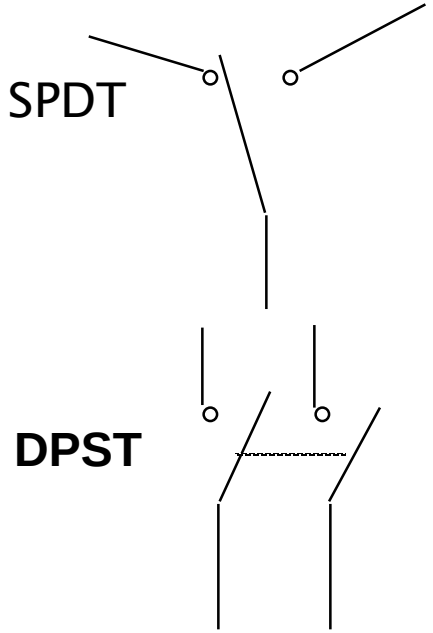


Make-before-break

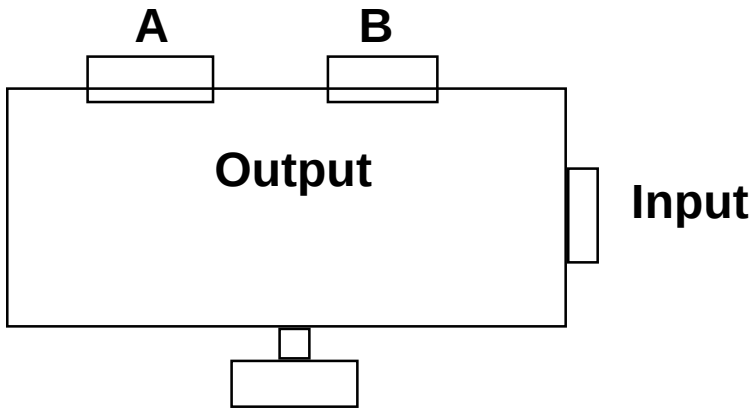
TERMS

Throw - number of states

Pole - number of connecting moving parts (number of individual circuits).

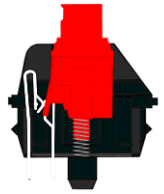


A serial switch box (A-B box) has two 25 pin serial ports to switch from.



How is this switch classified?

TYPES OF SWITCHES

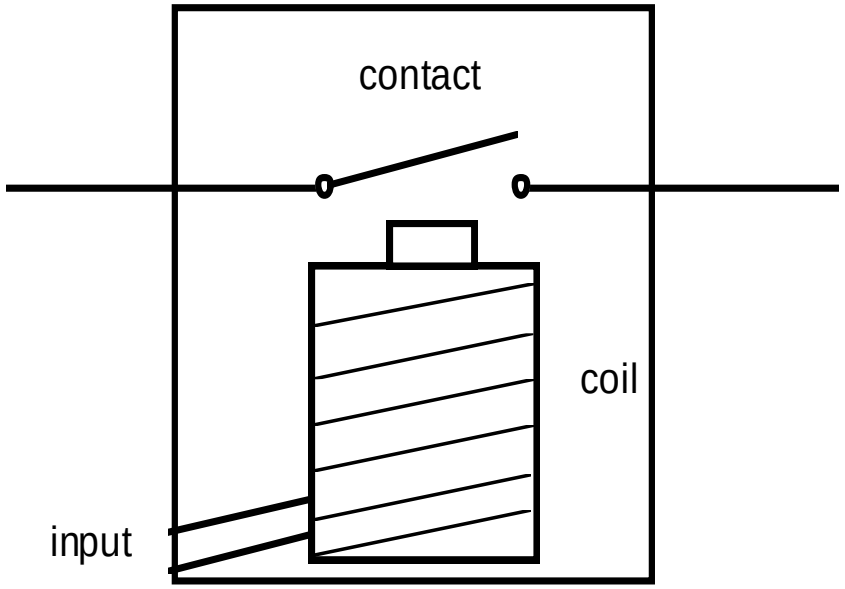


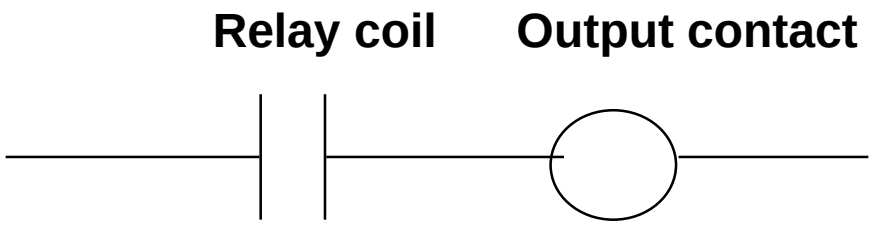
1. Basic switch, operated by a mechanical level,
2. Push-button switch,
3. Slide switch,
4. Thumbwheel switch,
5. Limit switch,
6. Proximity switch, and
7. Photoelectric switch.

RATING: voltage, current

RELAYS

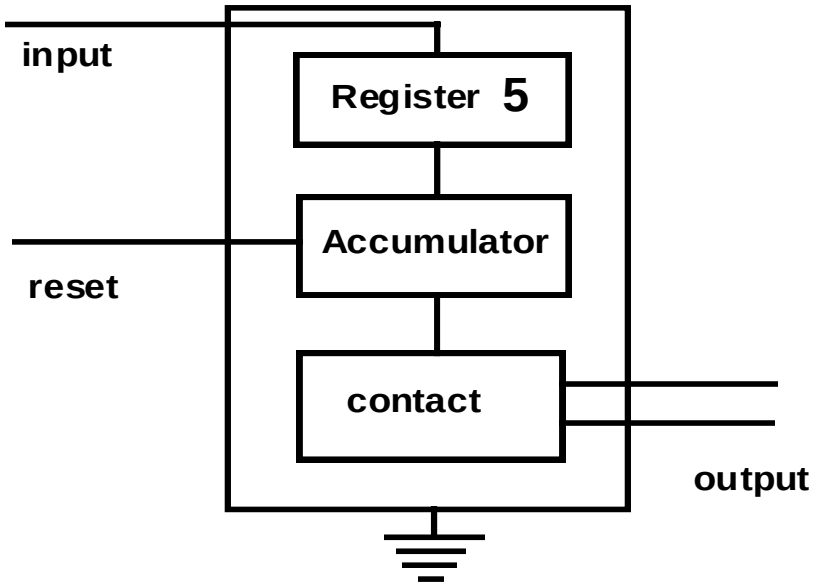
A switch whose operation is activated by an electromagnet is called a "relay"

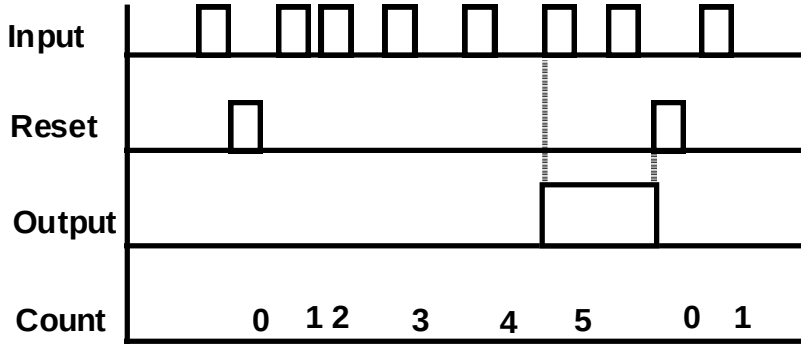




COUNTER

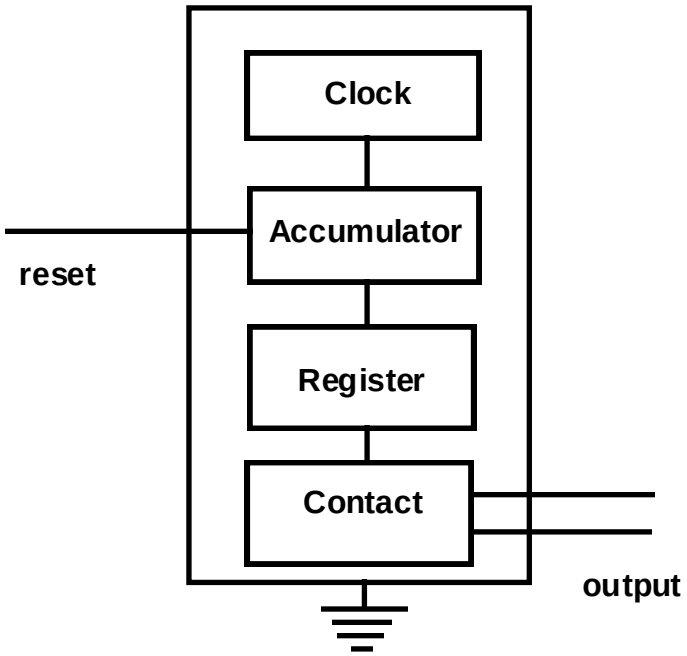
Digital counters output in the form of a relay contact when a preassigned count value is reached.

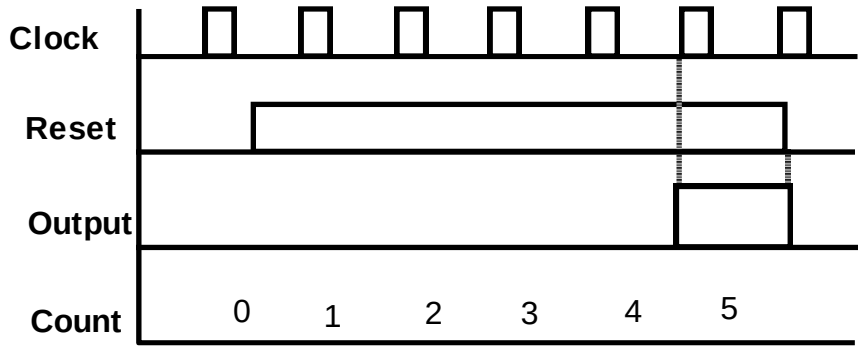




TIMER

A timer consists of an internal clock, a count value register, and an accumulator. It is used for or some timing purpose.

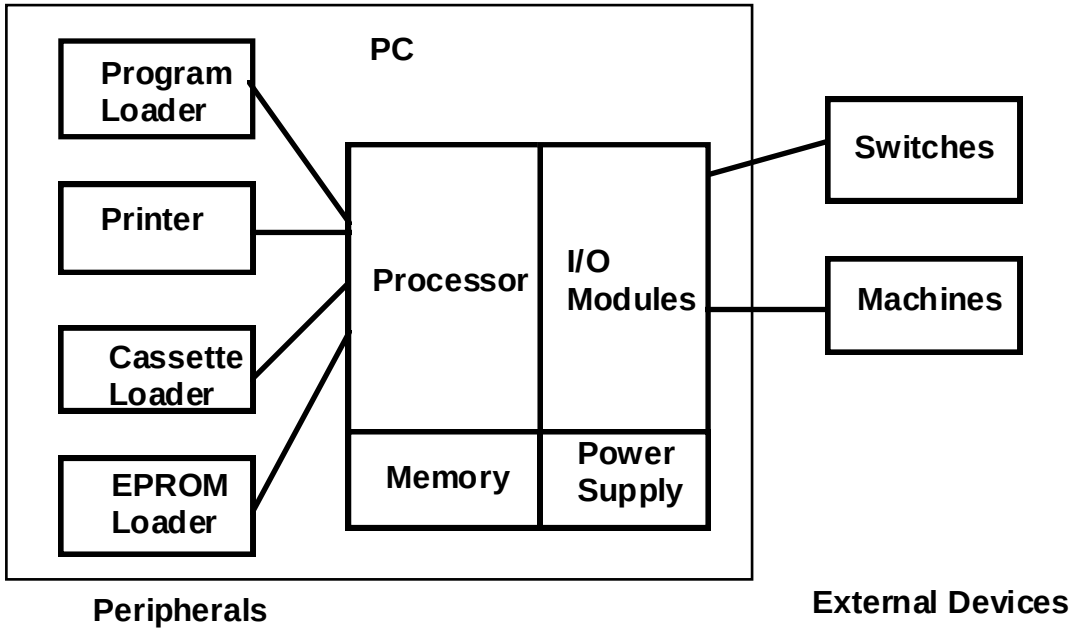




Time 5 seconds.

PLC ARCHITECTURE

Programmable controllers replace most of the relay panel wiring by software programming.



A typical PLC

PLC COMPONENTS

1. Processor

Microprocessor based, may allow arithmetic

operations, logic operators, block memory moves,

computer interface, local area network, functions, etc.

2. Memory

Measured in words.

ROM (Read Only Memory),

RAM (Random Access Memory),

PROM (Programmable Read Only Memory),

EEPROM (Electronically Erasable Programmable ROM),

EPROM (Erasable Programmable Read Only Memory),

EAPROM (Electronically Alterable Programmable Read Only Memory), and

some Additonal Memory.

PLC COMPONENTS

3. I/O

Modular plug-in periphery

AC voltage input and output,

DC voltage input and output,

Low level analog input,

High level analog input and output,

Special purpose modules, e.g.., high speed timers,

Stepping motor controllers, etc. PID, Motion

4. Power supply AC power

5. Peripheral

Hand held programmer (loader),

CRT programmer,

Operator console,

Printer,

Simulator,

EPROM loader,

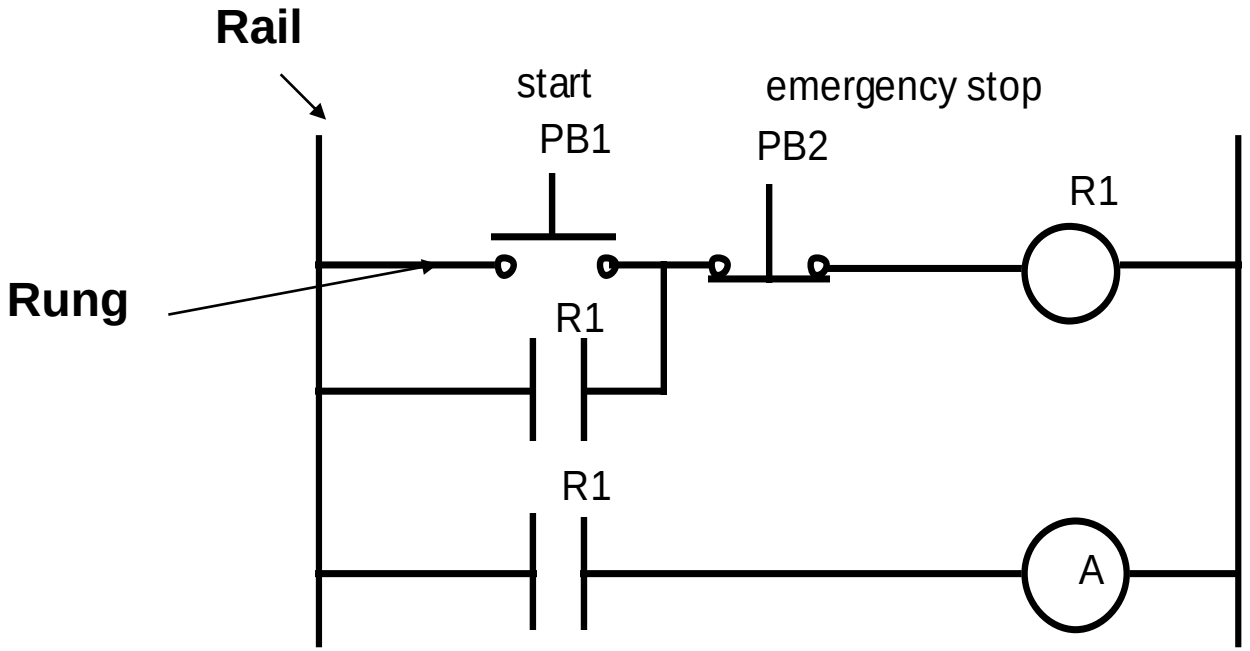
Cassette loader,

Graphics processor, and

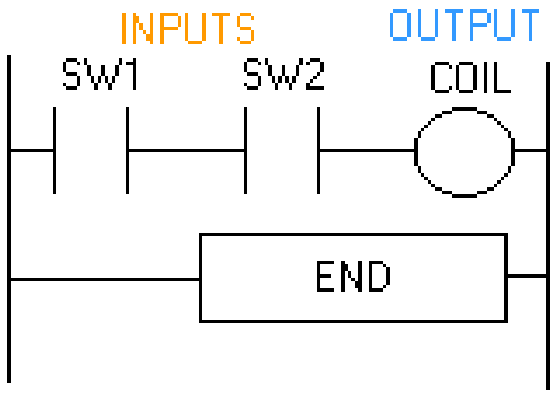
Network communication interface. MAP, LAN

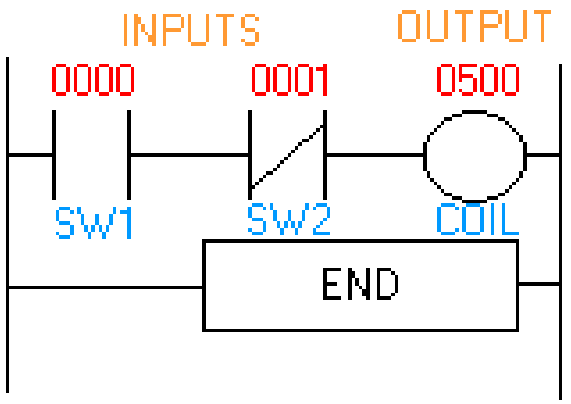
LADDER DIAGRAM

A ladder diagram (also called contact symbology) is a means of graphically representing the logic required in a relay logic system.



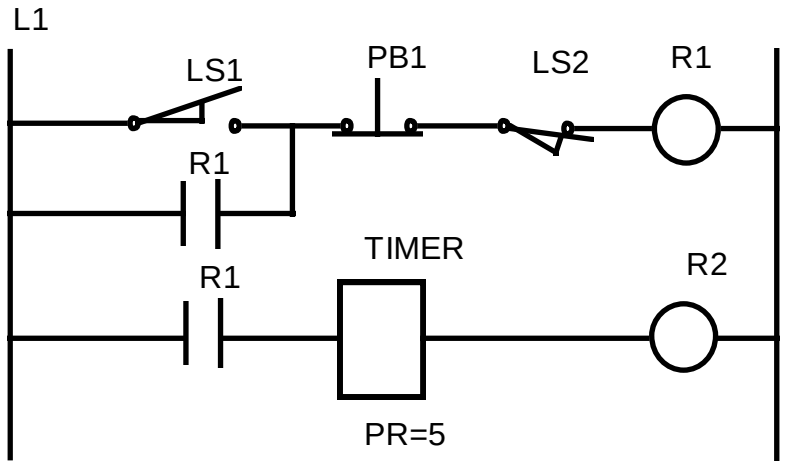
Ladder Representation

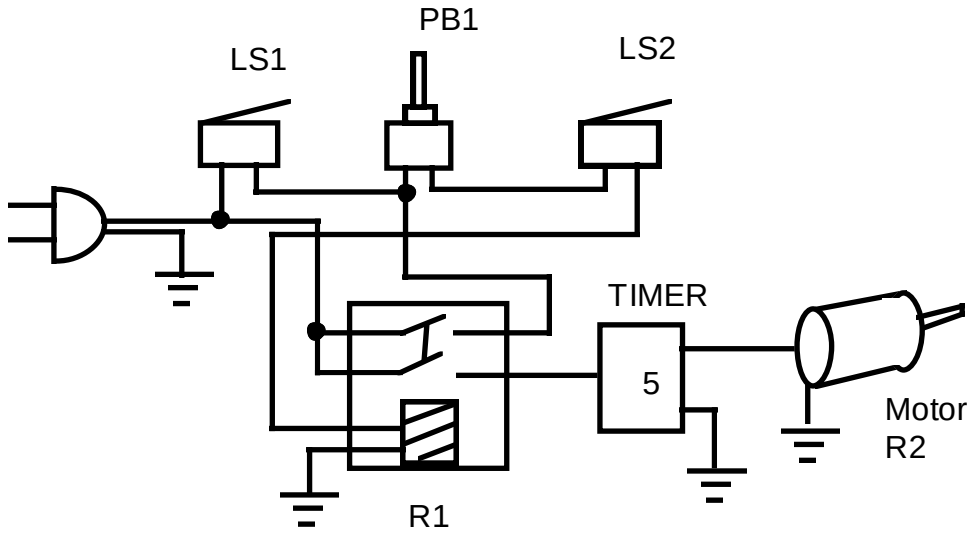




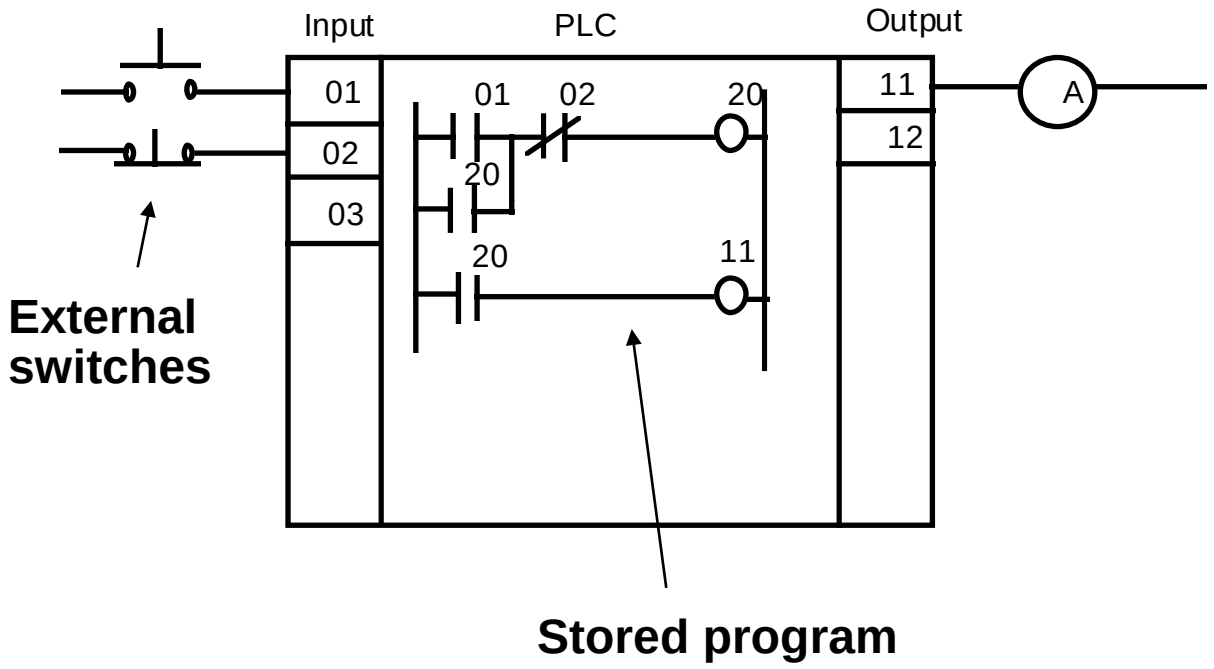
AN EXAMPLE OF RELAY LOGIC AND LADDER PROGRAM

For process control, it is desired to have the process start (by turning on a motor) five seconds after a part touches a limit switch. The process is terminated automatically when the finished part touches a second limit switch. An emergency switch will stop the process any time when it is pushed.



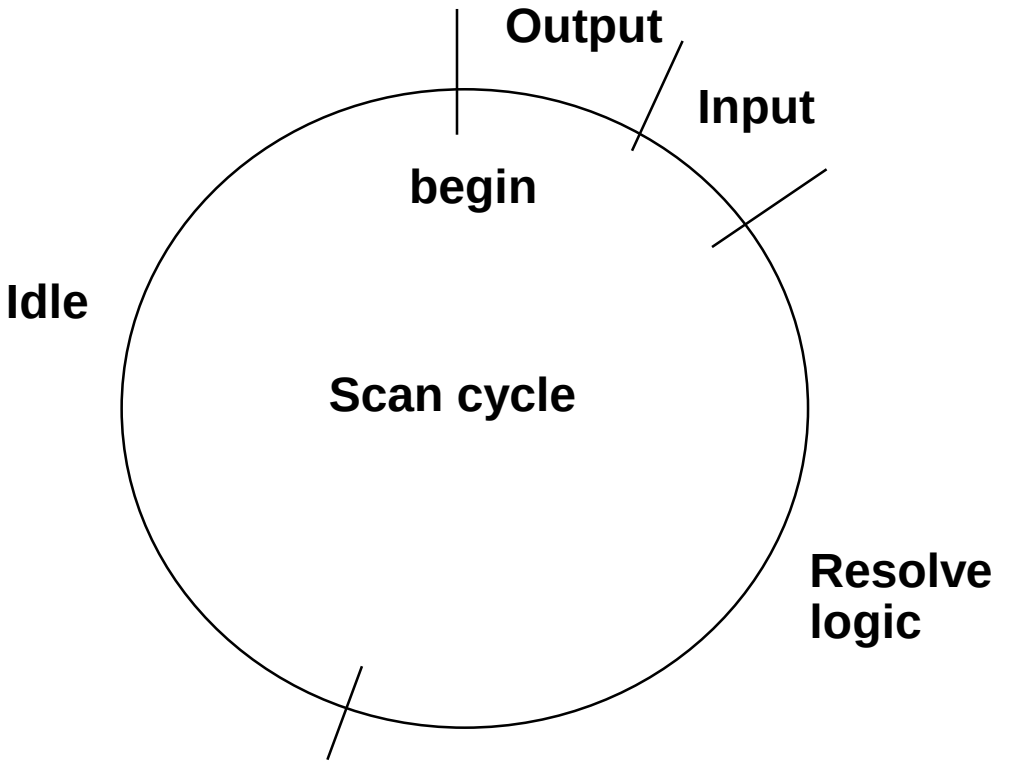


PLC WIRING DIAGRAM



SCAN

A PLC resolves the logic of a ladder diagram (program) rung by rung, from the top to the bottom. Usually, all the outputs are updated based on the status of the internal registers. Then the input states are checked and the corresponding input registers are updated. Only after the I/Os have been resolved, is the program then executed. This process is run in a endless cycle. The time it takes to finish one cycle is called the scan time.



PLC INSTRUCTIONS

1) Relay,
2) Timer and counter,
3) Program control,
4) Arithmetic,
5) Data manipulation,
6) Data transfer, and
7) Others, such as sequencers.

LOGIC STATES

ON : TRUE, contact closure, energize, etc.

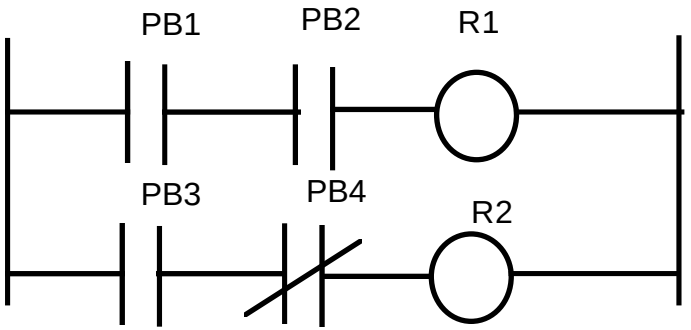
OFF: FALSE, contact open , de-energize, etc.

Do not confuse the internal relay and program with the external switch and relay. Internal symbols are used for programming. External devices provide actual interface.

(In the notes we use the symbol "~" to represent negation. AND and OR are logic operators.)

AND and OR LOGIC

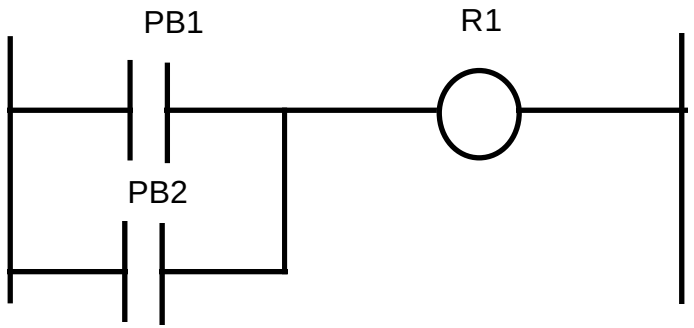
AND



R1 = PB1.AND.PB2

R2 = PB2.AND.~PB4

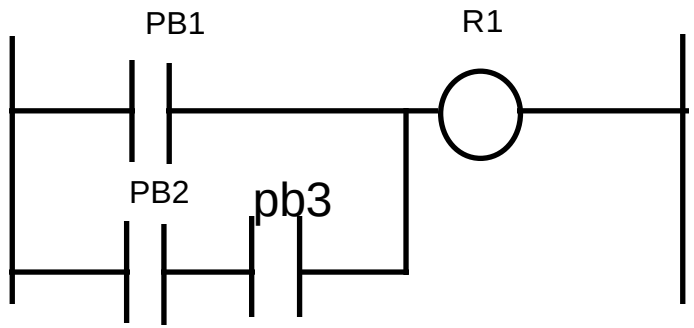
OR



R1 = PB1 .OR. PB2

COMBINED AND & OR

R1 = PB1 .OR. (PB2 .AND. PB3)



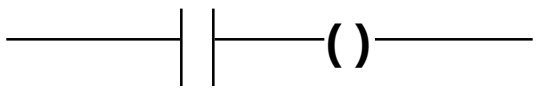
RELAY

A Relay consists of two parts, the coil and the contact(s).

Contacts:

a. Normally open -| |-
b. Normally closed -|/|-
c. Off-on transitional -|↑|-
d. On-off transitional -|↓ |-

Coil:



a. Energize Coil -( )-
b. De-energize -(/)-
c. Latch -(L)-
d. Unlatch -(U)-

TIMERS AND COUNTERS

Timers:

a. Retentive on delay -(RTO)-

b. Retentive off delay -(RTF)-

c. Reset -(RST)-

	Input		
	True	False	True
RTO	counting	stop	counting resume
RTF	stop	counting	stop

RTO reach PR value, output ON
RTF reach PR value, output OFF

PR value in 0.1 second

Counter:

a. Counter up -(CTU)-

b. Counter down -(CTD)-

c. Counter reset -(CTR)-

SEQUENCER

Sequencers are used with machines or processes involving repeating operating cycles which can be segmented into steps.

	Output			
Step	A	B	C	Dwell time
1	ON	OFF	OFF	5 sec.
2	ON	ON	OFF	10 sec.
3	OFF	OFF	ON	3 sec.
4	OFF	ON	OFF	9 sec.

Rockwell/ Allen Bradley PLC

I/O points are numbered, they correspond to the I/O slot on the PLC.

For A-B controller used in our lab

I/O uses 1-32

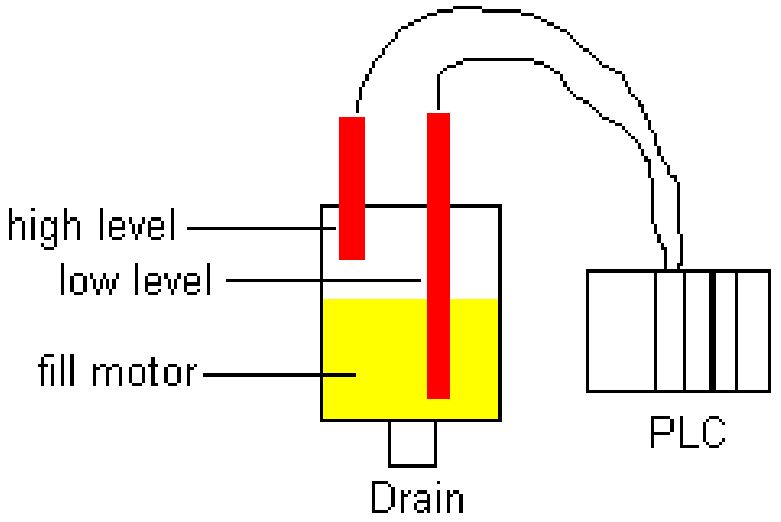
Internal relays use 033 - 098

Internal timers/counters/sequencers use 901-932

Status 951-982

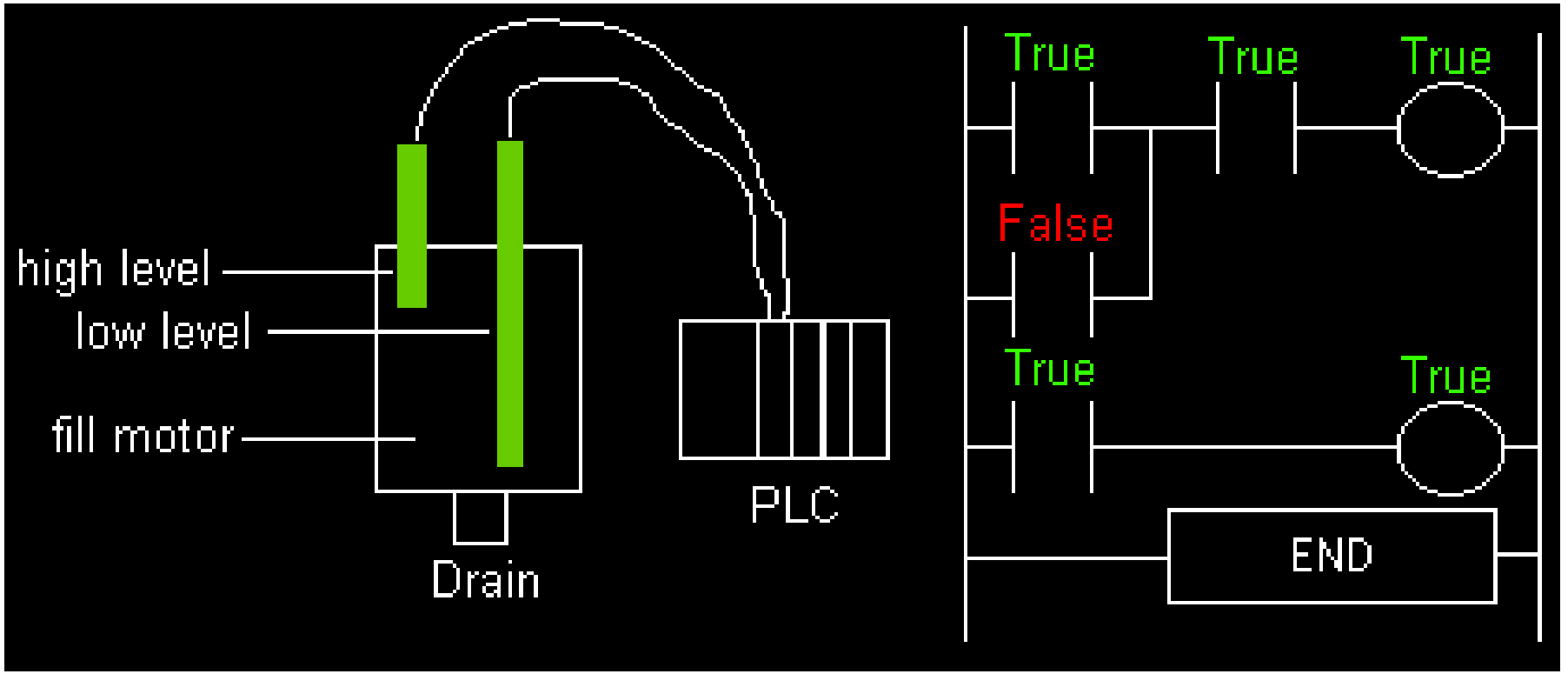
Programming a PLC

Oil is consumed randomly. The tank needs to be refilled by turning on a pump. Two hydrostatic switches are used to detect a high and low level.



Dispensing oil from a tank

How does it work?



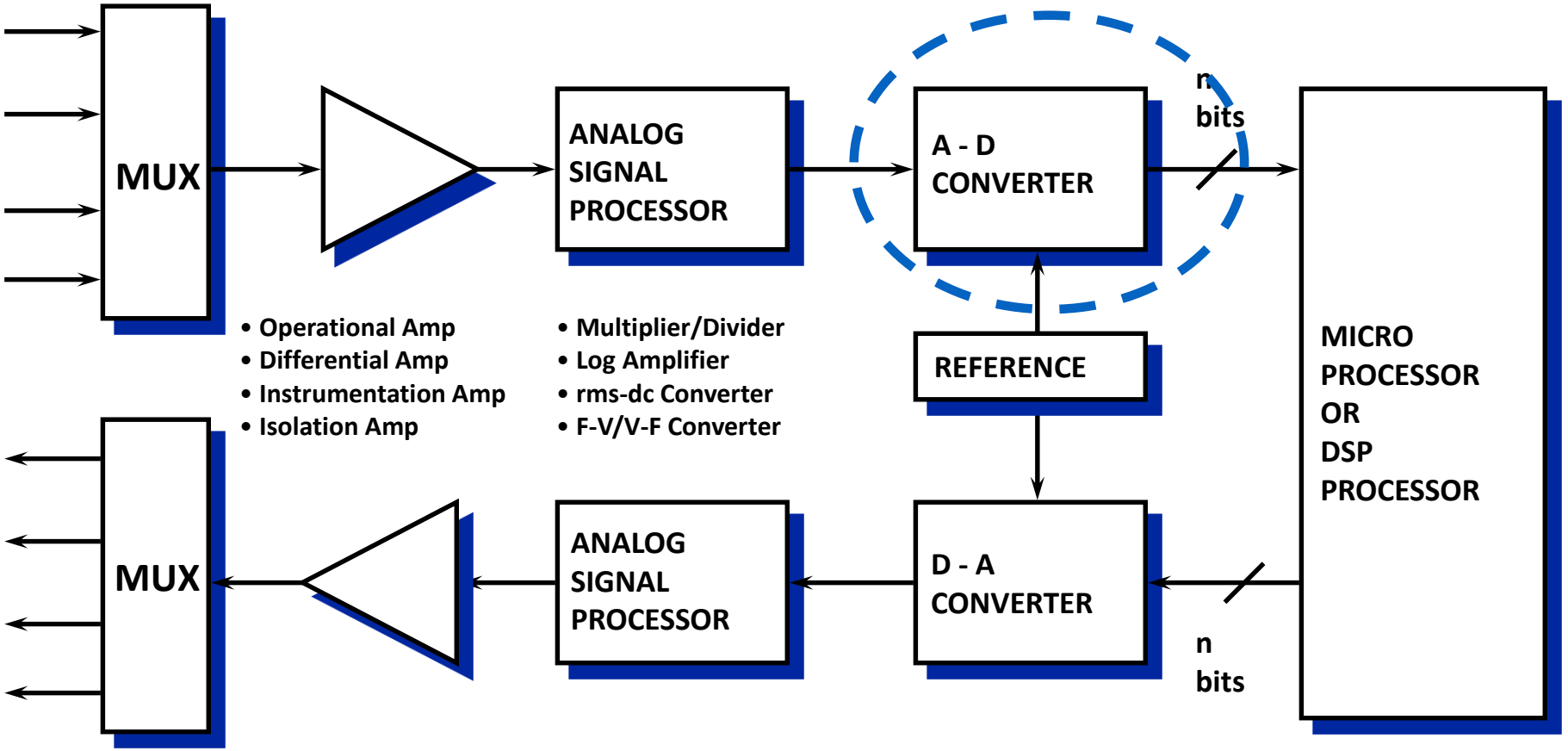
Signal Converters

- Analog to Digital
- Digital to Analog

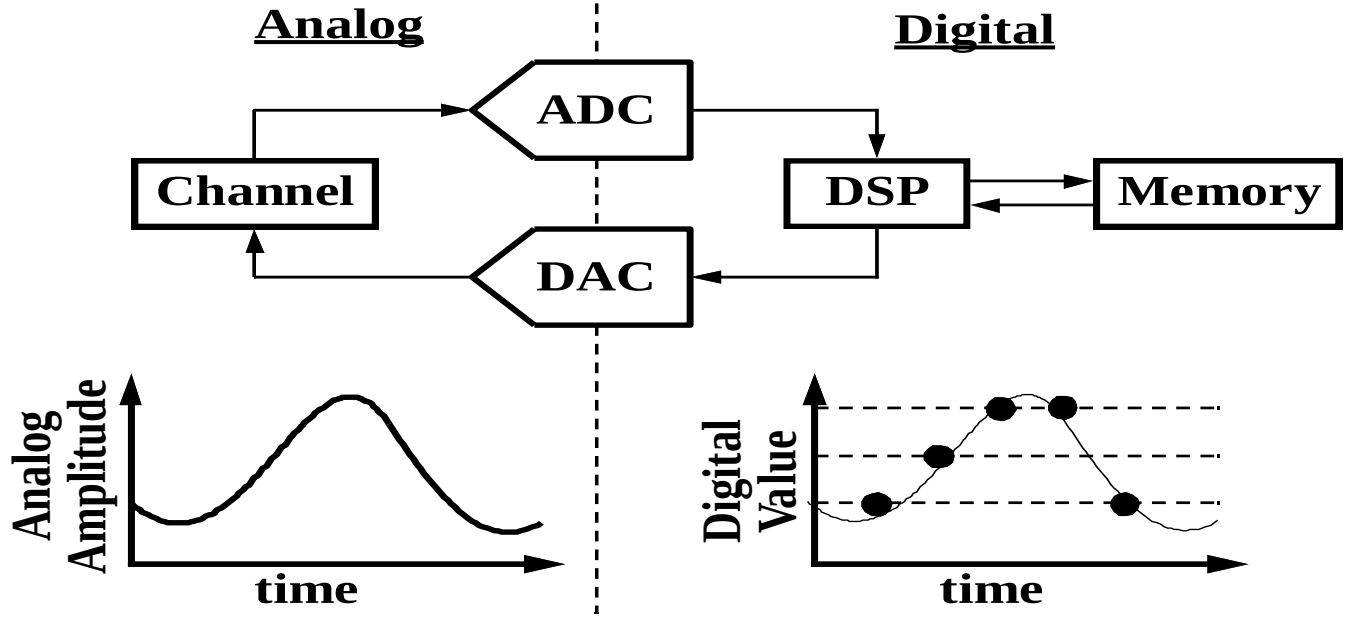
A/D Converter (ADC) Introduction

- A/D Fundamentals
  - Sampling
  - Quantization
- Factors Affecting A/D Converter Performance
  - Static Performance
  - Dynamic Performance
- ADC Architectures
  - SAR ADCs
  - Pipelined ADCs
  - Flash Type ADC
  - Sigma-Delta ADCs
- High Speed ADC Application Considerations

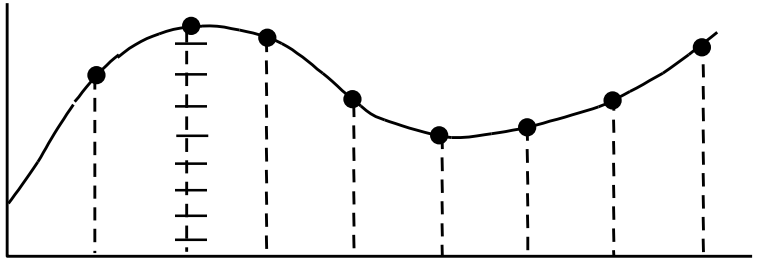
The Measurement & Control Loop



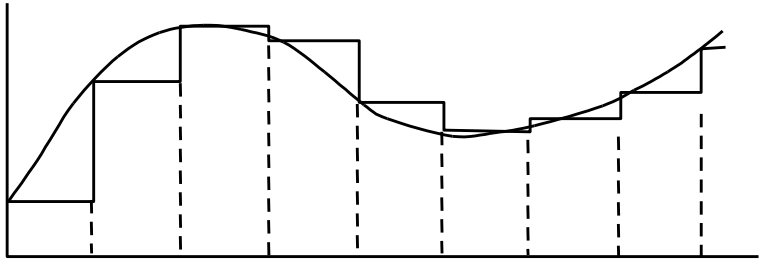
“REAL WORLD” SAMPLED DATA SYSTEMS CONSIST OF ADCs and DACs



ADC SAMPLED AND QUANTIZED WAVEFORM



DAC RECONSTRUCTED WAVEFORM



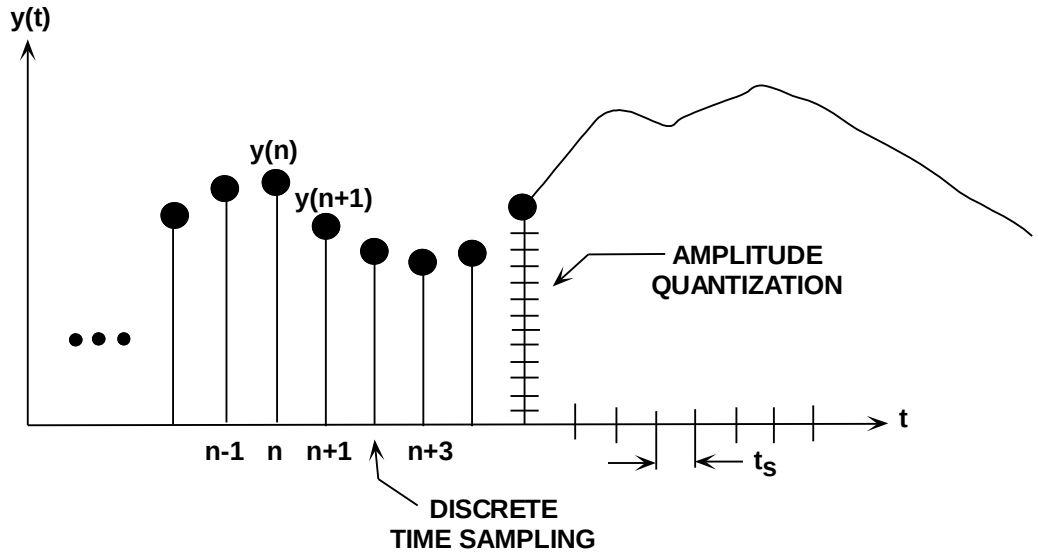
What is an Analog-Digital Converter?

$$\text{DIGITAL OUTPUT CODE} = \frac{\text{Analog Input}}{\text{Reference Input}} \times (2^N - 1)$$

- Produces a Digital Output Corresponding to the Value of the Signal Applied to Its Input Relative to a Reference Voltage
- Finite Number of Discrete Values : 2^N Resulting in Quantization Uncertainty
- Changes Continuous Time Signal into Discrete Time Sampled Representation
- Sampling and Quantization Impose Fundamental yet Predictable Limitations

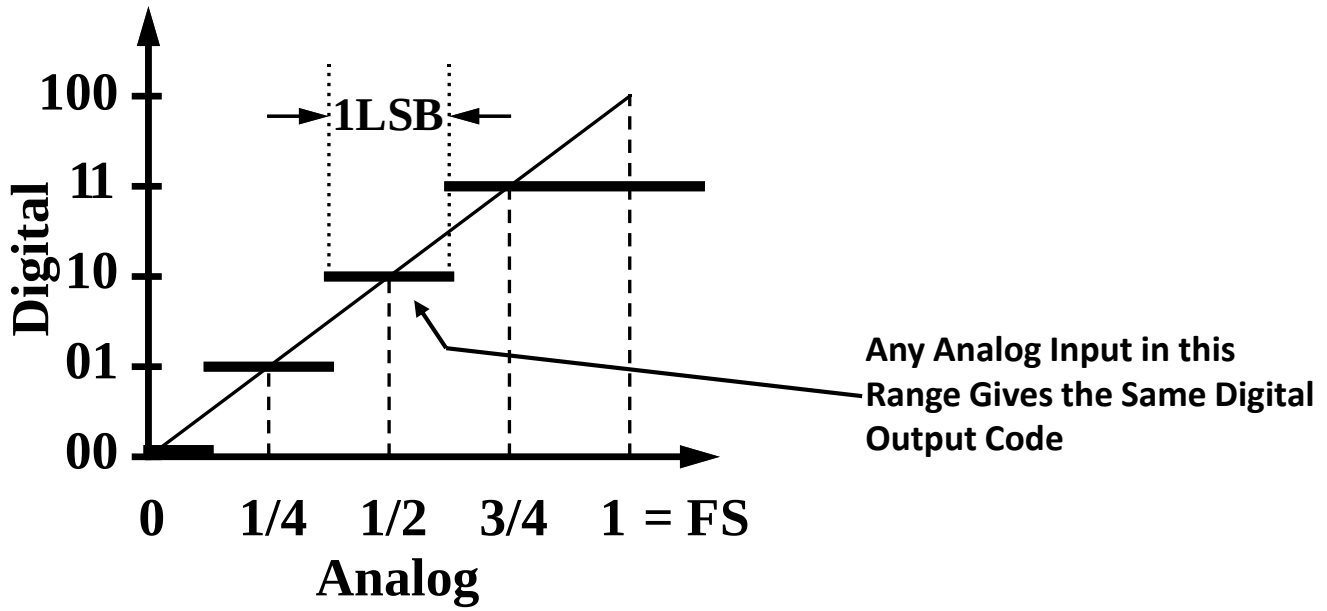
Sampling Process

- Representing a continuous time domain signal at discrete and uniform time intervals
- Determines maximum bandwidth of sampled (ADC) or reconstructed (DAC) signal (Nyquist Criteria)
- Frequency Domain- "Aliasing" for an ADC and "Images" for a DAC

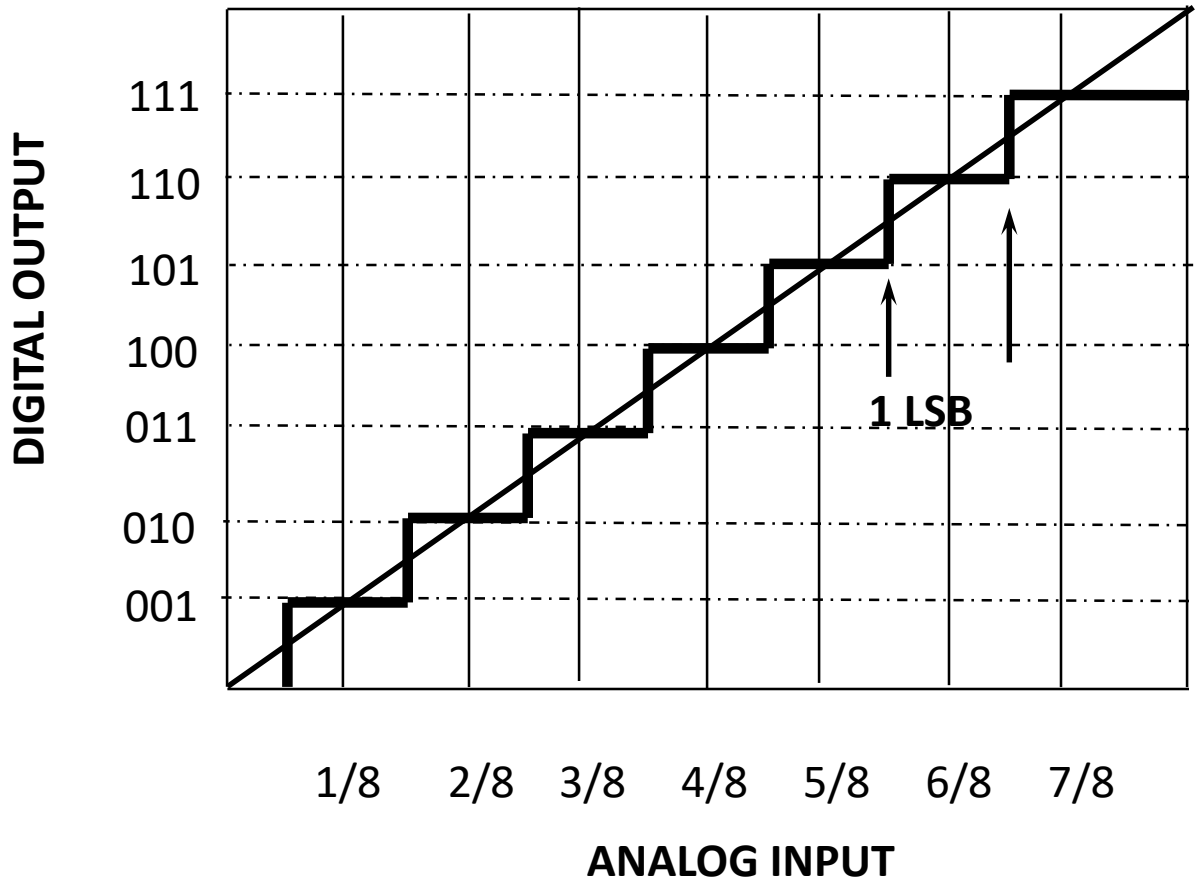


Quantization Process

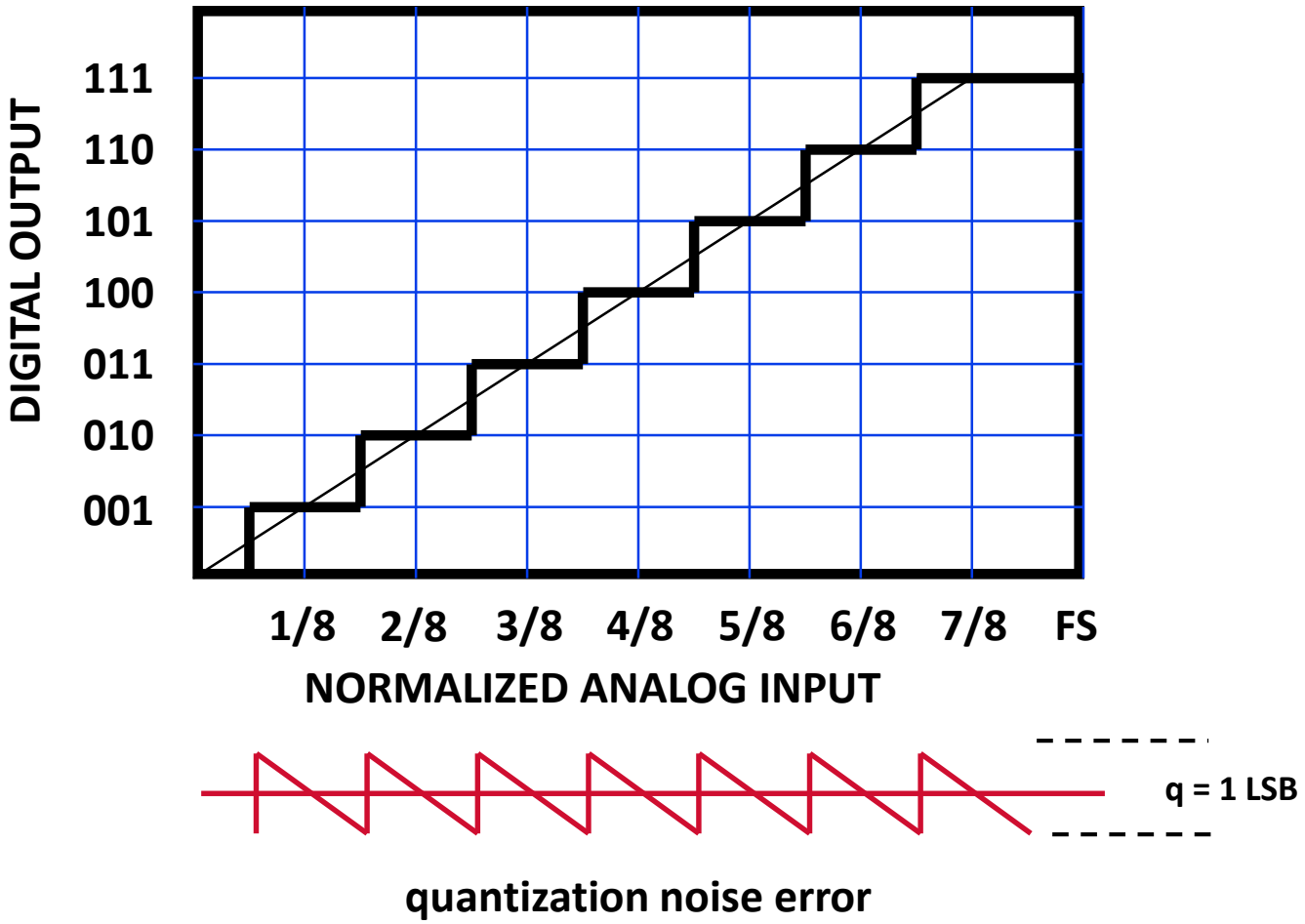
- Quantization Process
  - Representing an analog signal having infinite resolution with a digital word having finite resolution
  - Determines Maximum Achievable Dynamic Range
  - Results in Quantization Error/Noise



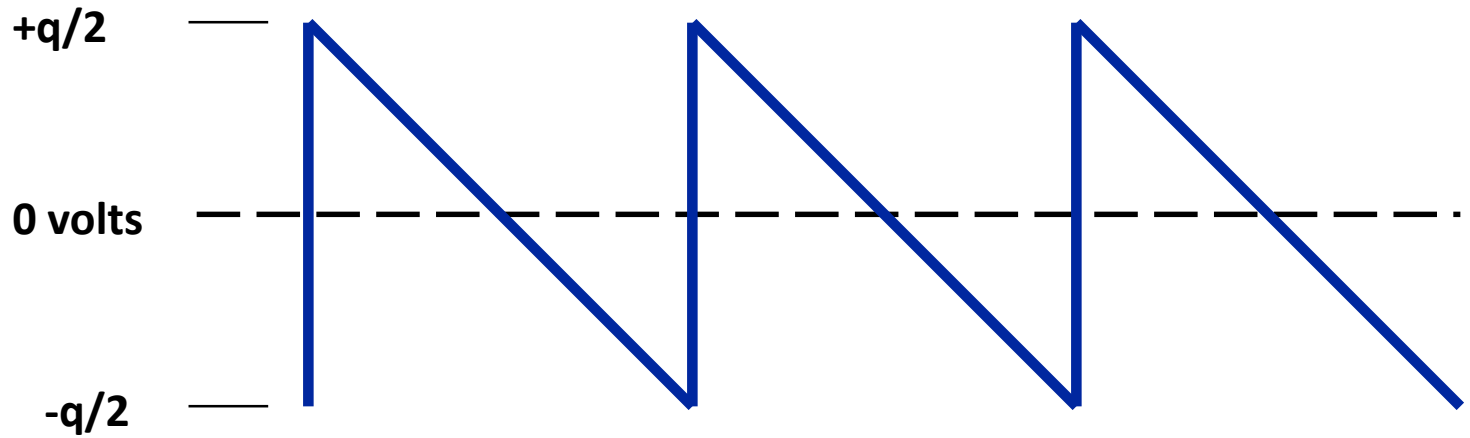
Conversion Relationship for an Ideal A/D Converter



Quantization Noise

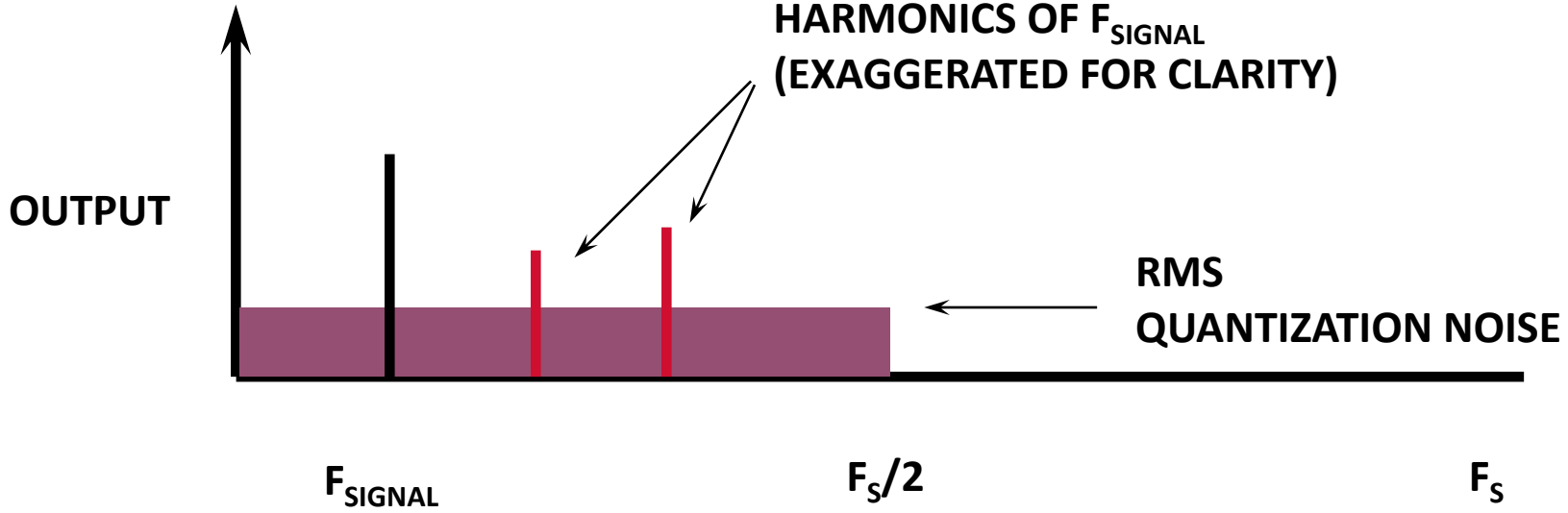


Quantization Noise (con't)



- The RMS value of the quantization noise sawtooth is its peak value, q÷2, divided by $\sqrt{3}$, or q ÷ $\sqrt{12}$
- For Sine Wave Full Scale RMS Value is $2^{(N-1)}/\sqrt{2}$
- For Saw Tooth Quantization Error Signal RMS Value is q /$\sqrt{12}$
- Thus S/N is 1.225 x 2^N
- Expressed in dB as 1.76 + 6.02N, where N is the resolution of the A/D converter

Quantization Noise (con't)



- **If the quantization noise is uncorrelated with the frequency of the AC input signal, the noise will be spread evenly over the Nyquist bandwidth of $F_s/2$.**
- **If, however the input signal is locked to a sub-multiple of the sampling frequency, the quantization noise will no longer appear uniform, but as harmonics of the fundamental frequency**

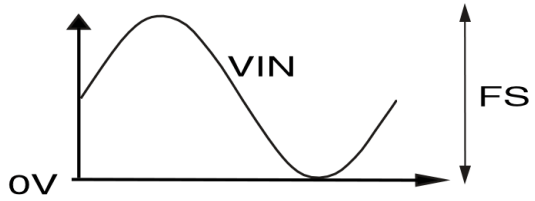
ADC Resolution vs. Quantization Parameters

Resolution, Bits (n)	2^n	LSB, mV (2.5V FS)	% Full Scale	ppm Full Scale	dB Full Scale
8	256	9.77	0.391	3906	-48.0
10	1024	2.44	0.098	977	-60.0
12	4096	0.610	0.024	244	-72.0
14	16,384	0.153	0.006	61	-84.0
16	65,536	0.038	0.0015	15	-96.0
18	262,164	0.0095	0.00038	3.8	-108.0

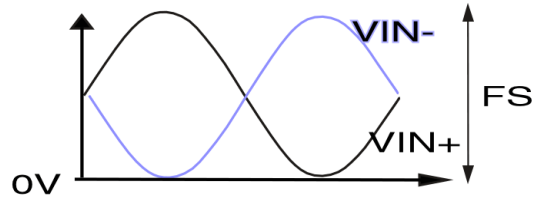
Analog Input Signal Definitions

FS - FULL SCALE

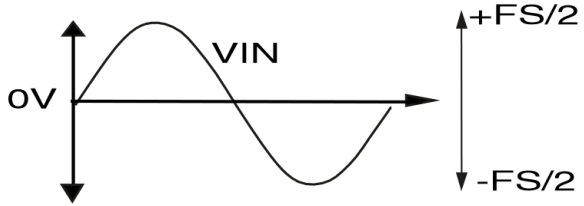
(1) UNIPOLAR SINGLE ENDED



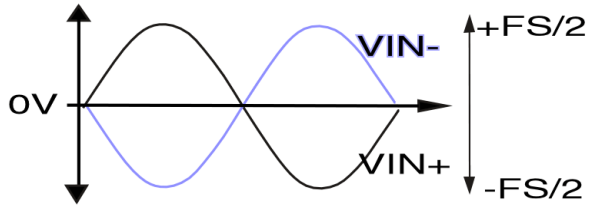
(2) UNIPOLAR DIFFERENTIAL



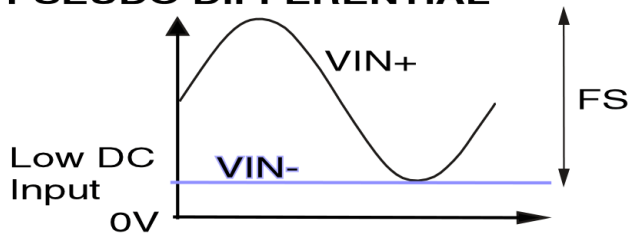
(3) BIPOLAR SINGLE ENDED



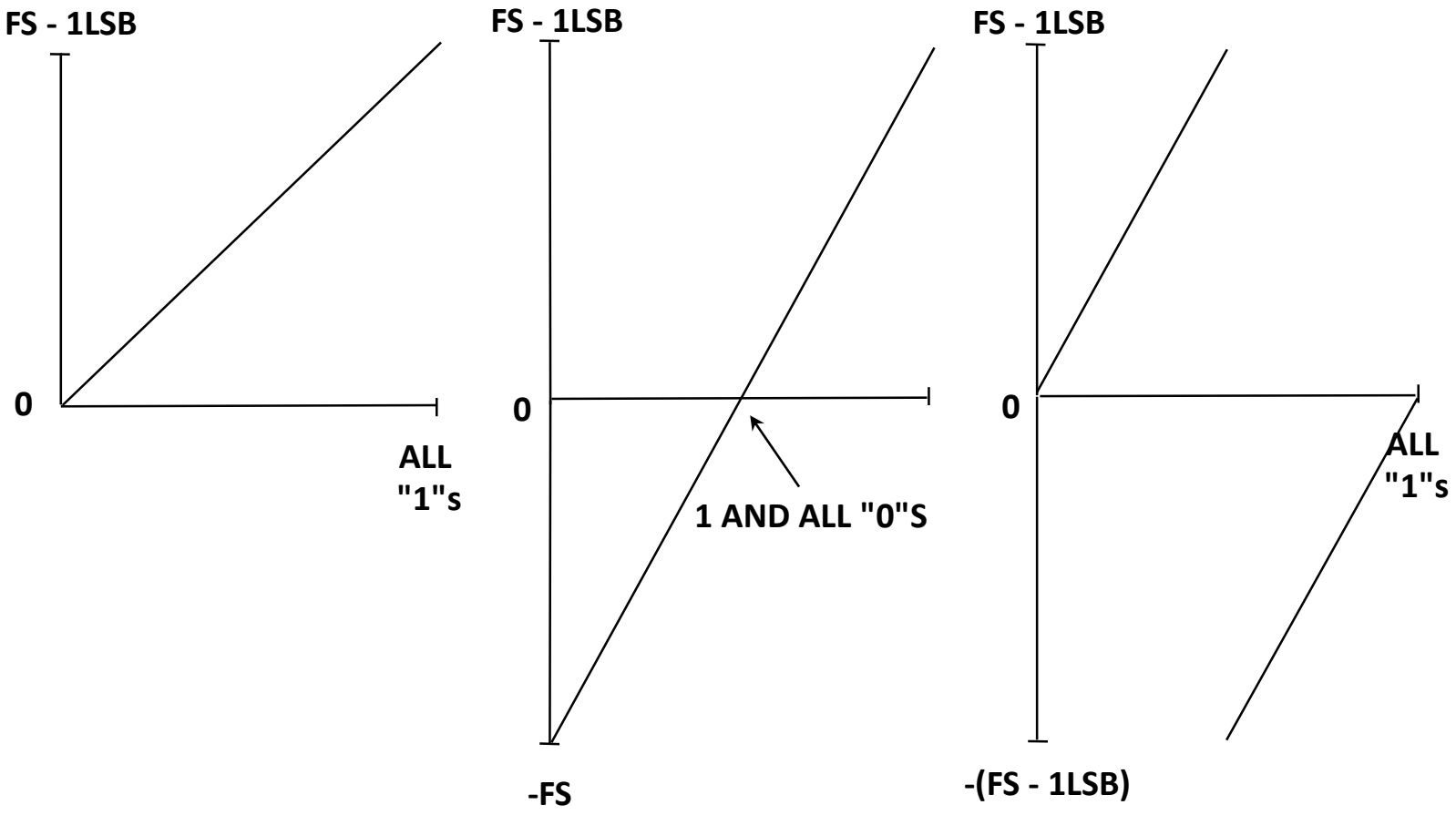
(4) BIPOLAR DIFFERENTIAL



(5) PSEUDO DIFFERENTIAL

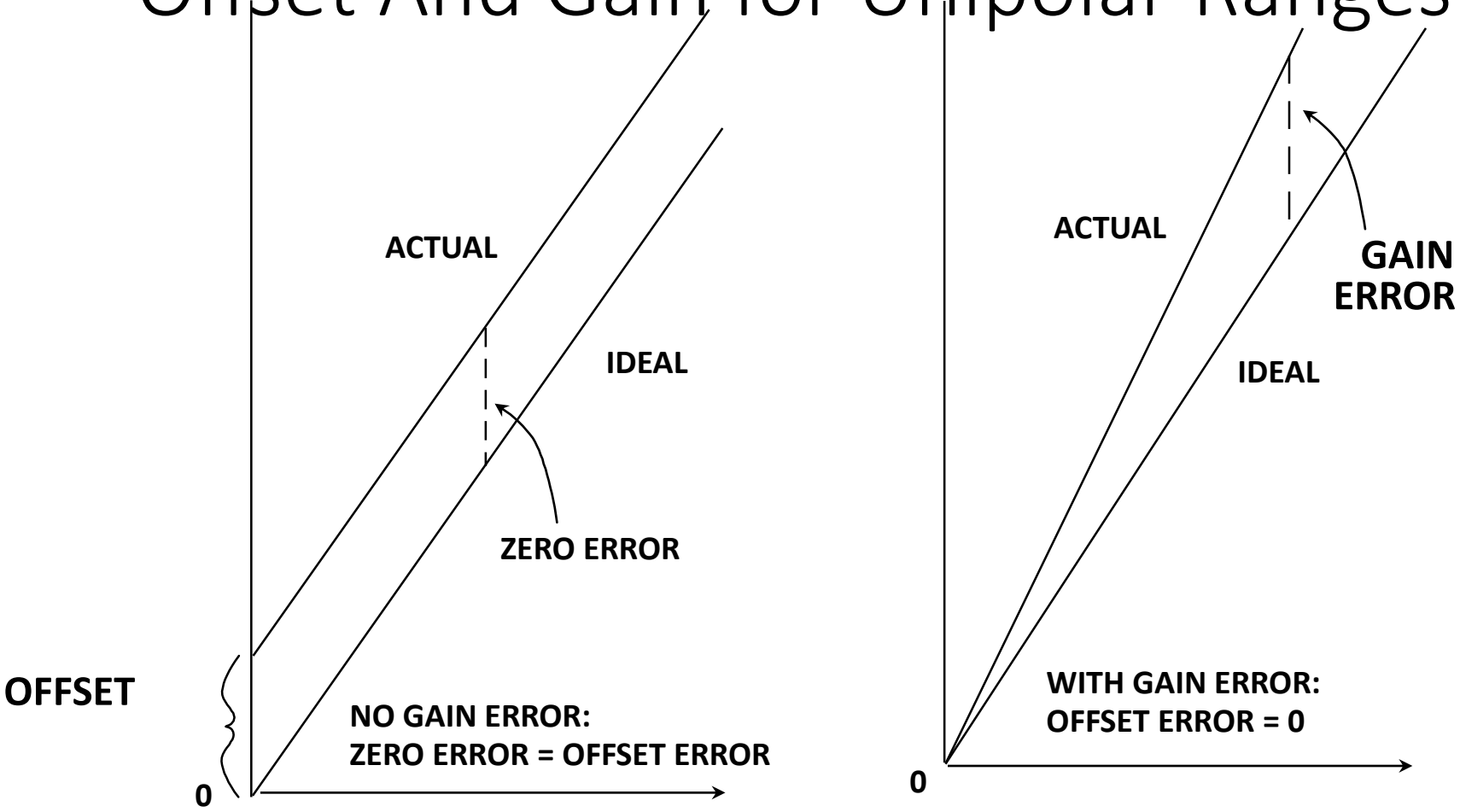


Unipolar and Bipolar Converter Codes

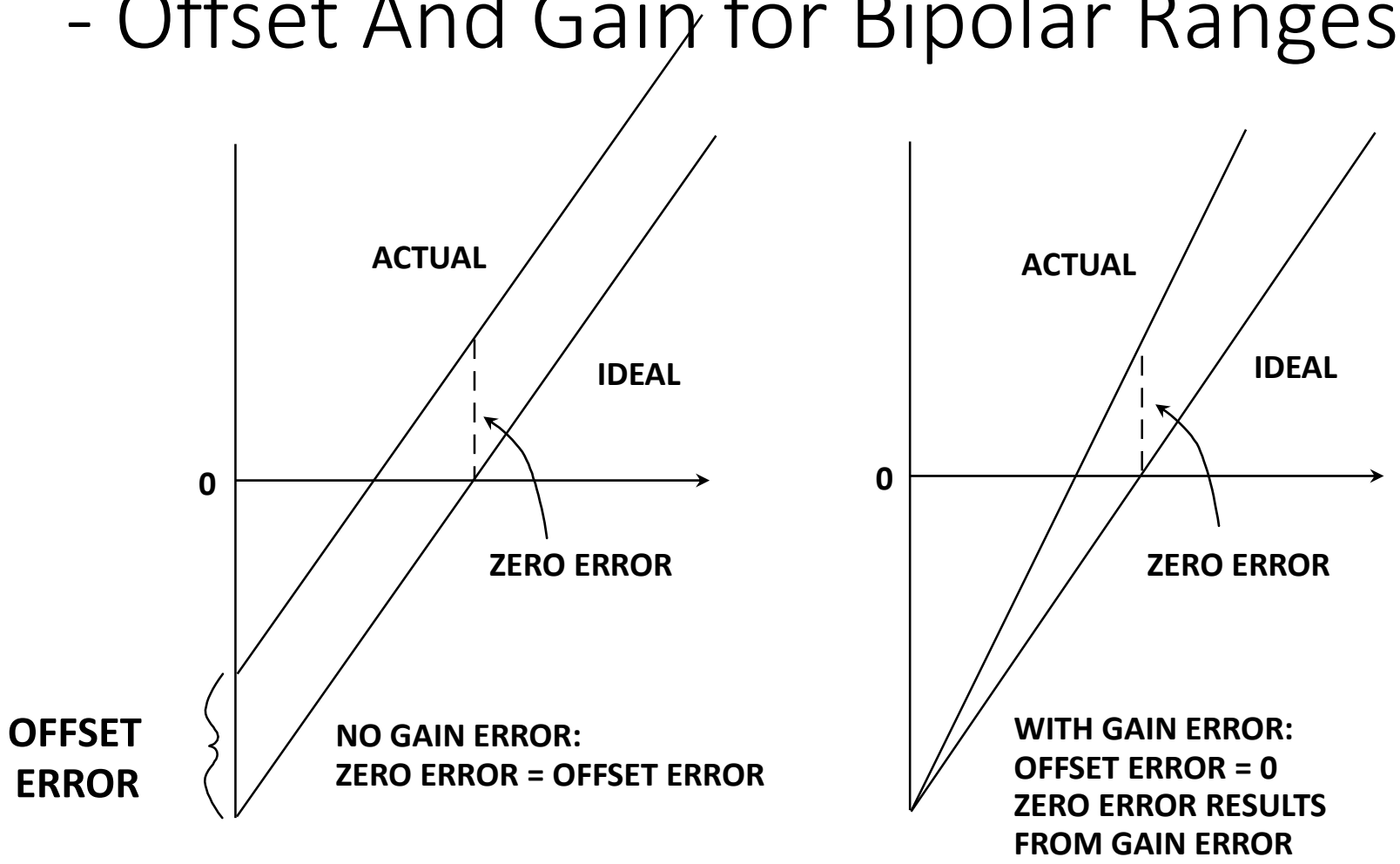


UNIPOLAR **OFFSET BINARY** **2's COMPLEMENT**

Factors Affecting A/D Converter Performance
- Offset And Gain for Unipolar Ranges

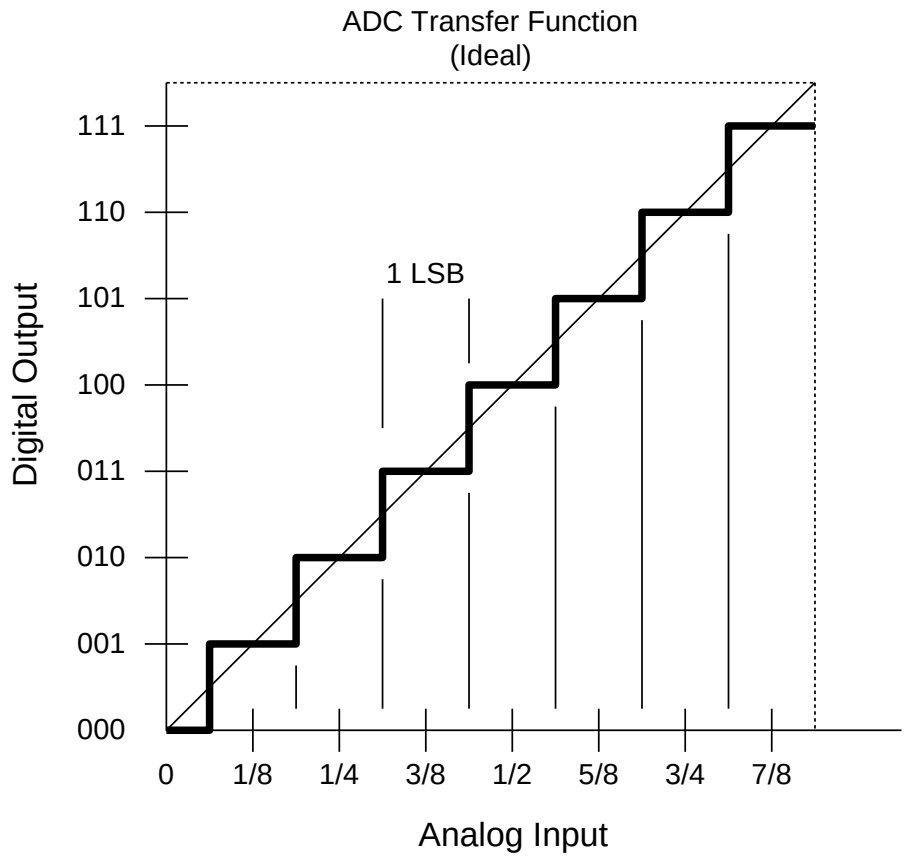


Factors Affecting A/D Converter Performance
- Offset And Gain for Bipolar Ranges



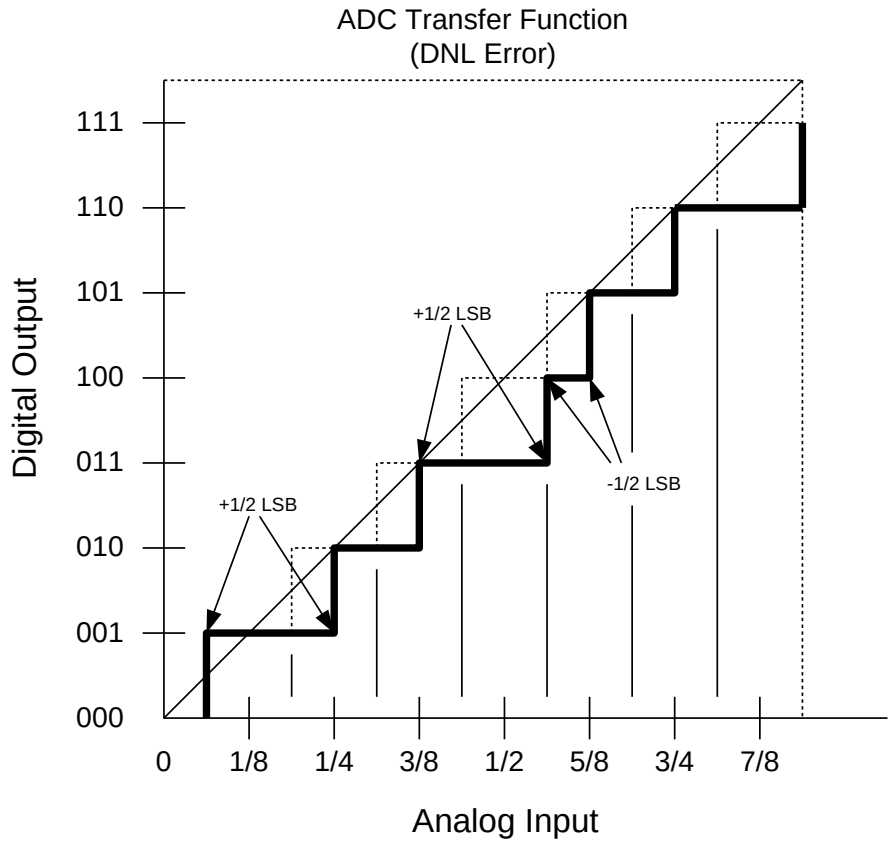
DC Specifications (Ideal)

- Ideal ADC code transitions are exactly 1 LSB apart.
- For an N-bit ADC, there are 2^N codes. (1 LSB = FS/ 2^N)
- For this 3-bit ADC, 1 LSB = ($1V/2^3$ = 1/8th)
- Each “step” is centered on an eighth of full scale



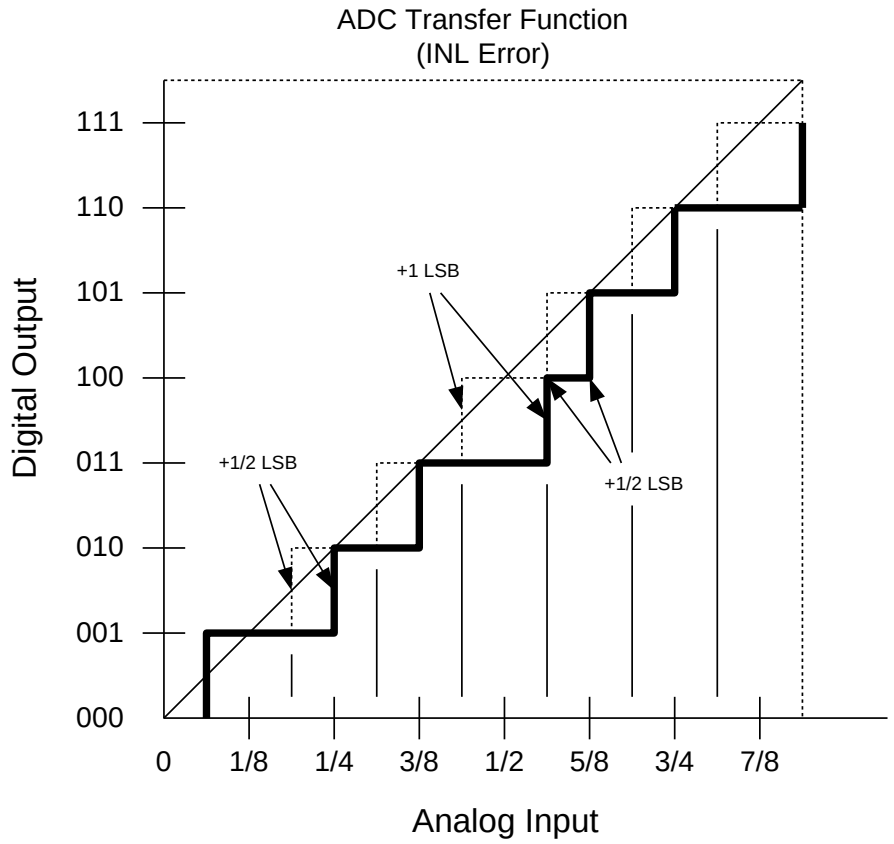
DC Specifications (DNL)

- Differential Non-Linearity (DNL) is the deviation of an actual code width from the ideal 1 LSB code width
- Results in narrow or wider code widths than ideal and can result in missing codes
- Results in additive noise/spurs beyond the effects of quantization



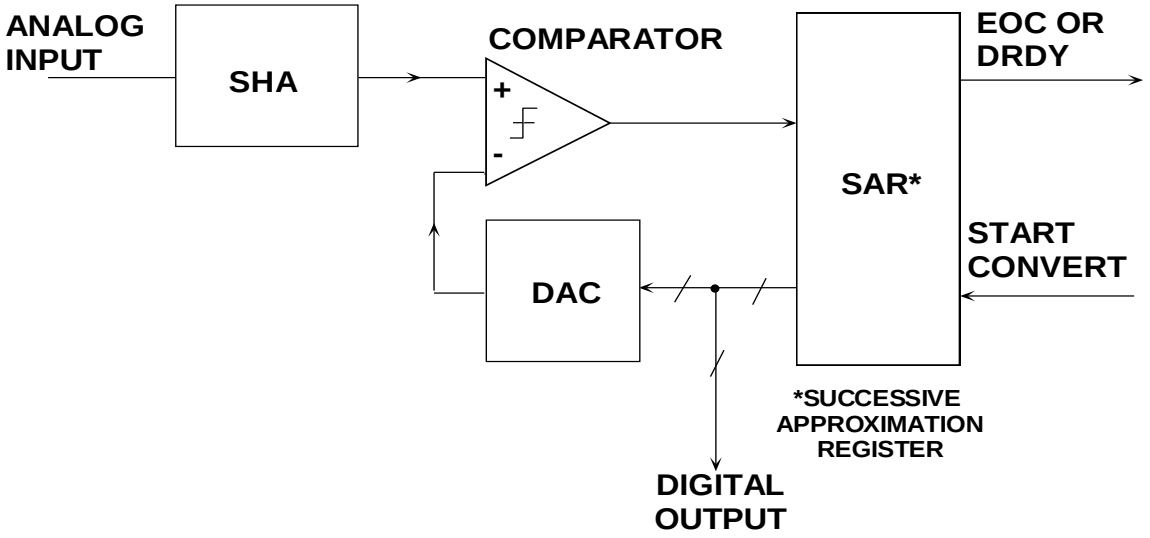
DC Specifications (INL)

- Integral Non-Linearity (INL) is the deviation of an actual code transition point from its ideal position on a straight line drawn between the end points of the transfer function.
- INL is calculated after offset and gain errors are removed
- Results in additive harmonics and spurs

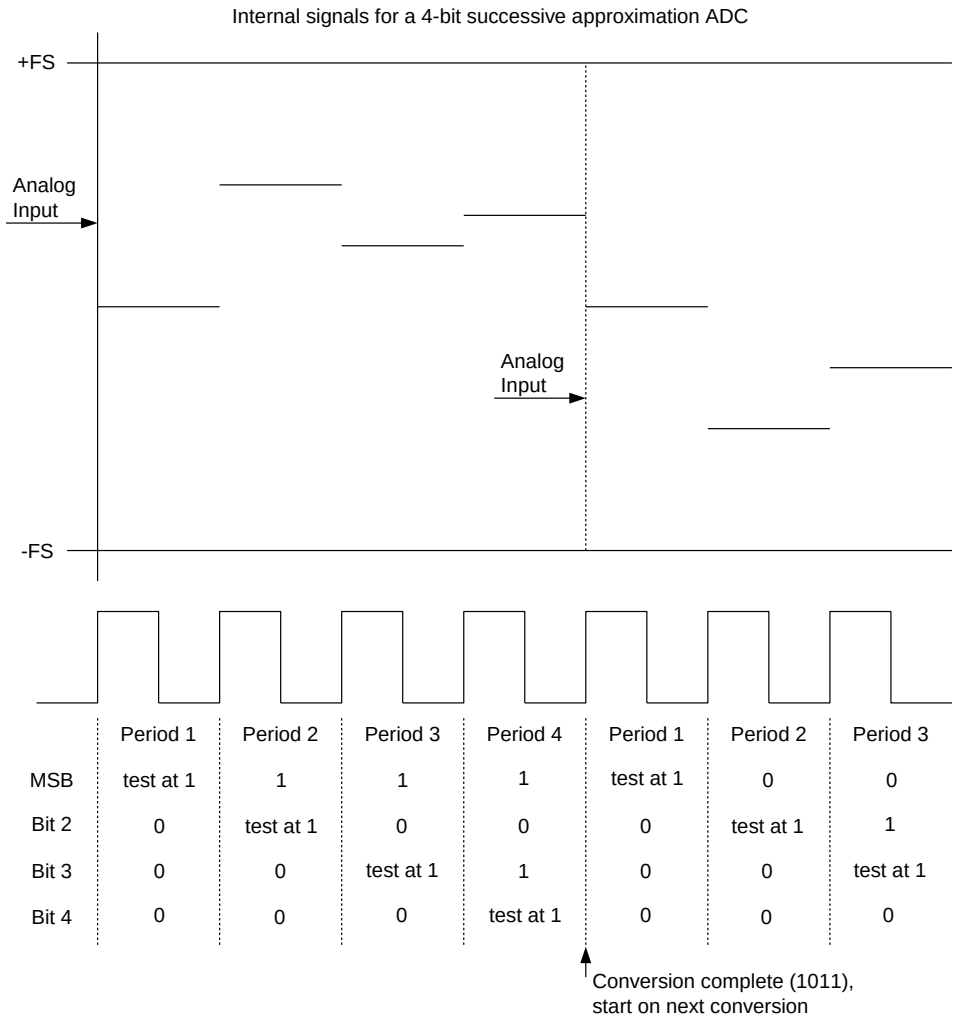


Successive Approximation ADC

"Recursive" One-Bit Sub-Ranging Architecture



Successive Approximation ADC



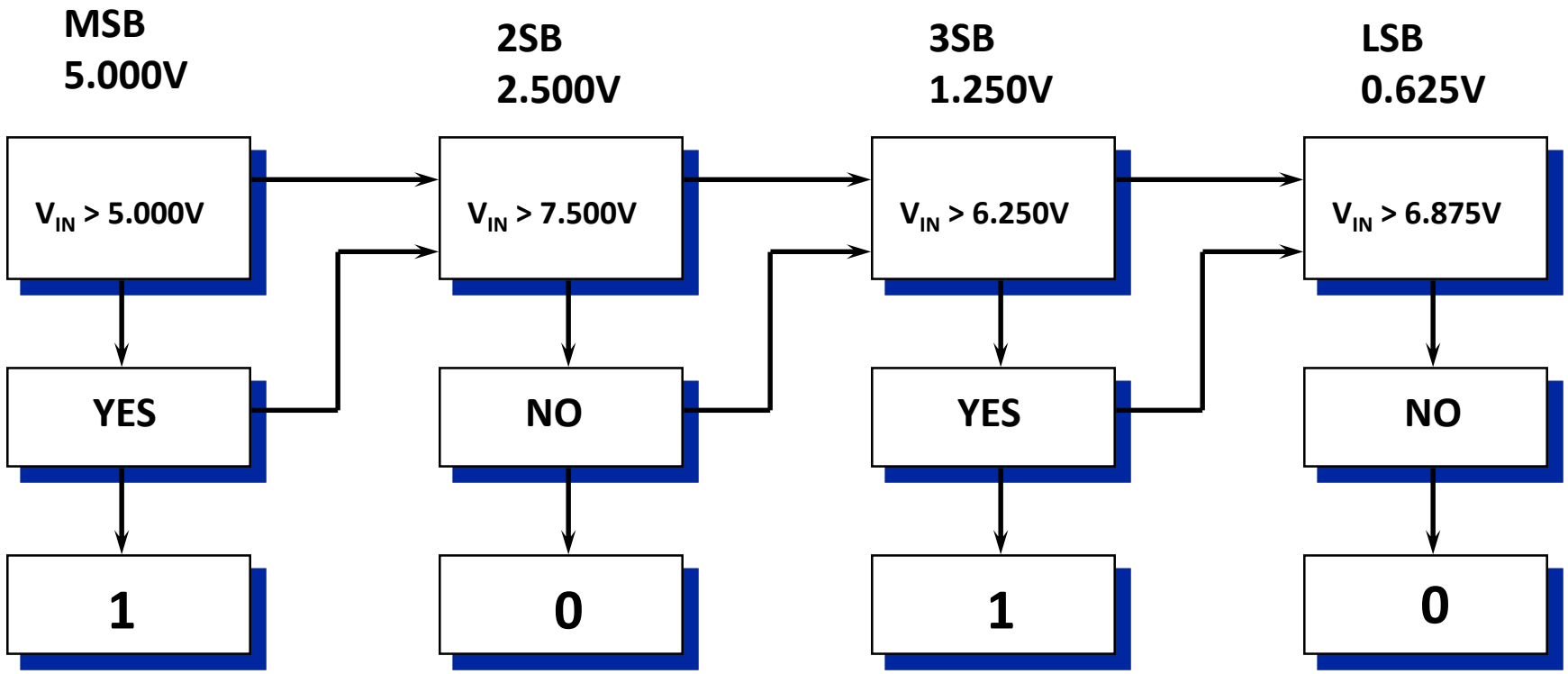
	Period 1	Period 2	Period 3	Period 4	Period 1	Period 2	Period 3
MSB	test at 1	1	1	1	test at 1	0	0
Bit 2	0	test at 1	0	0	0	test at 1	1
Bit 3	0	0	test at 1	1	0	0	test at 1
Bit 4	0	0	0	test at 1	0	0	0

How a Successive Approximation A/D Converter Works

- Rising/Falling Edge of Convert Start Pulse Resets Logic
- Falling/Rising Edge Begins Conversion Process
- Bit Comparisons Made on Each Clock Edge
- Conversion Time Equals Number of Comparisons (Resolution) Times Clock Period
- The Accuracy of Conversion Depends on the DAC Linearity and Comparator Noise

How Successive Approximation Works

EXAMPLE : ANALOG INPUT = 6.428V, REFERENCE = 10.000V



Successive Approximation ADC

Advantages to SAR A/D converters

- Low Power (12-bit/1.5 MSPS ADC: 1.7 mW)
- Higher resolutions (16-bit/1 MSPS)
- Small Die Area and Low Cost
- No pipeline delay

Tradeoffs to SAR A/D converters

- Lower sampling rates

Typical Applications

- Instrumentation
- Industrial control
- Data acquisition

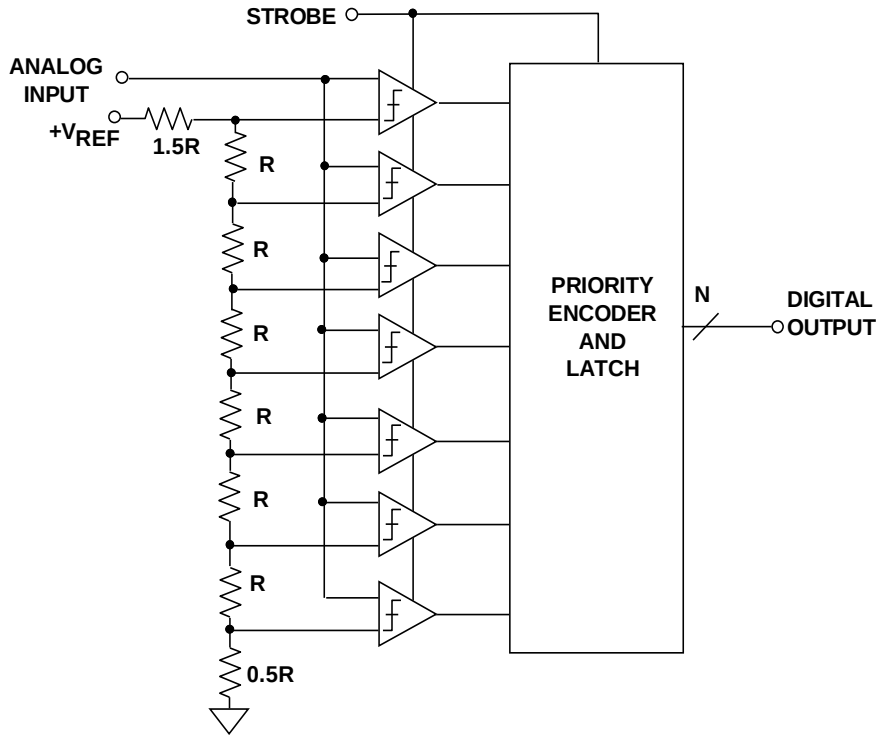
Flash or Parallel ADC

2N-1 comparators form the digitizer array, where N is the ADC resolution

Analog input is applied to one side of the comparator array, a 1 lsb reference ladder voltage is applied to the other inputs.

The comparator array is clocked simultaneously and decides in parallel.

Output logic converts from thermometer code to binary



Flash or Parallel ADC

Advantages to Flash A/D converters

- Fastest conversion times (up to 1 GSPS)
- Low data latency

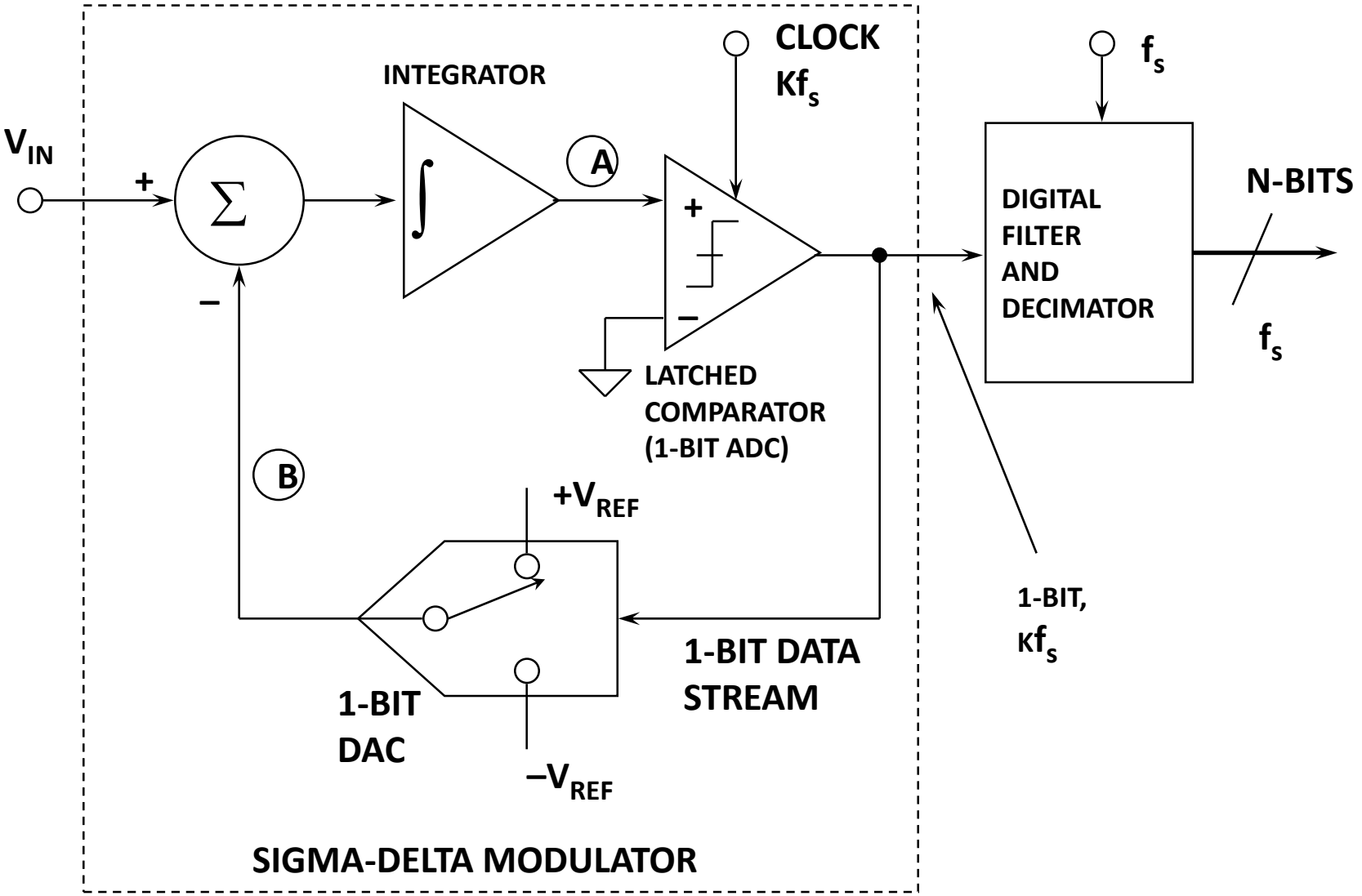
Tradeoffs to Flash A/D converters

- Higher power consumption
- High capacitive input is difficult to drive

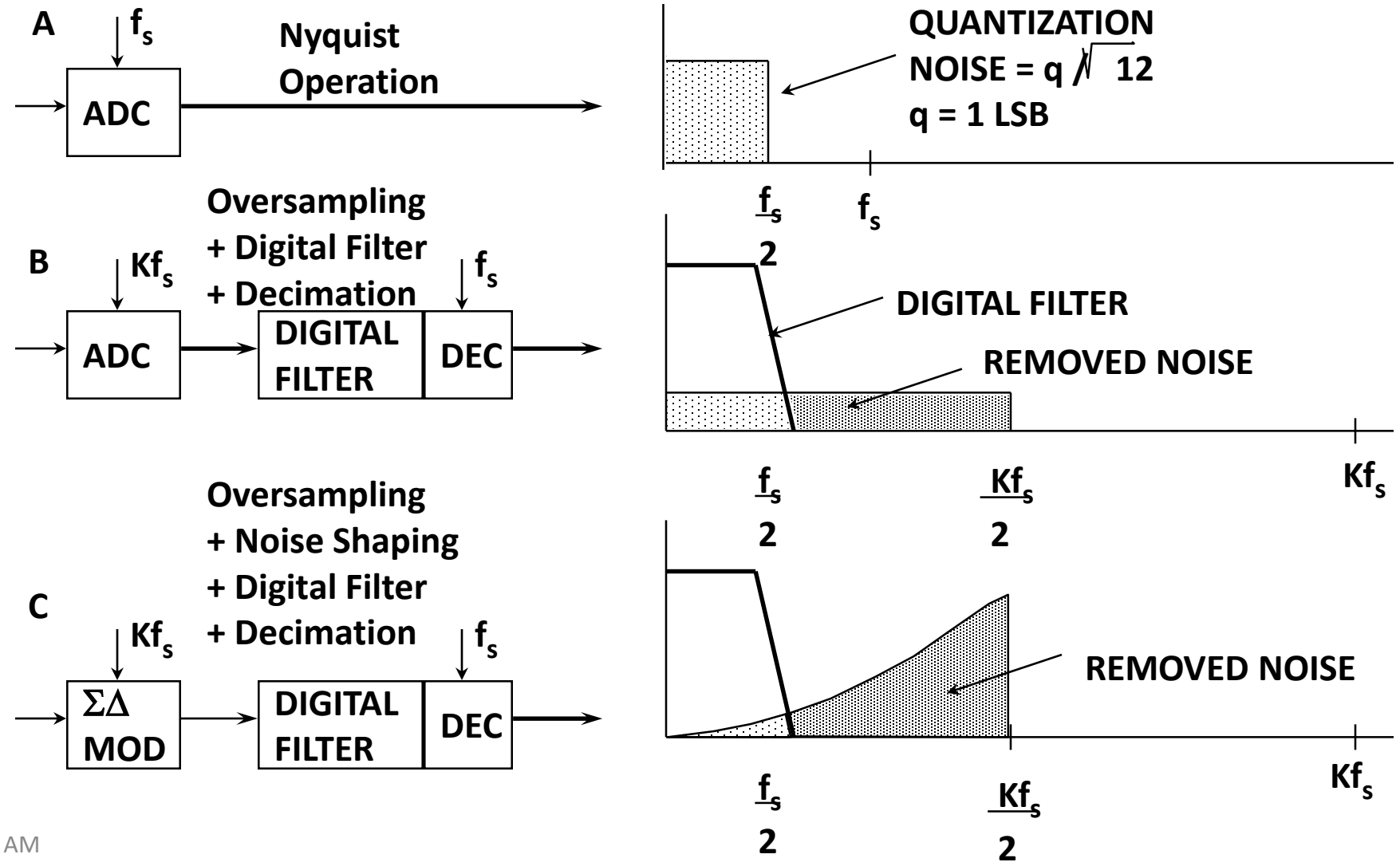
Typical Applications

- Video digitization
- High-speed data acquisition

FIRST-ORDER SIGMA-DELTA ADC



OVERSAMPLING, DIGITAL FILTERING, NOISE SHAPING, AND DECIMATION



DEFINITION OF "NOISE-FREE" CODE RESOLUTION

- **EFFECTIVE RESOLUTION** $= \log_2 \left[\frac{\text{FULLSCALE RANGE}}{\text{RMS NOISE}} \right]$ **BITS**
- **NOISE-FREE CODE RESOLUTION** $= \log_2 \left[\frac{\text{FULLSCALE RANGE}}{\text{P-P NOISE}} \right]$ **BITS**

P-P NOISE = 6.6 × RMS NOISE

- **NOISE-FREE CODE RESOLUTION** $= \log_2 \left[\frac{\text{FULLSCALE RANGE}}{6.6 \times \text{RMS NOISE}} \right]$ **BITS**

20mV

16.5bits

0.4uVrms

= EFFECTIVE RESOLUTION – 2.72 BITS

SIGMA-DELTA ADCs

Advantages to Sigma-Delta A/D converters

- High resolutions and accuracy (24-bits)
- Excellent DNL and INL performance
- Noise shaping capability

Tradeoffs in Sigma-Delta A/D converters

- Limited input bandwidth
- Slower sampling rates

Typical Applications

- Precision data acquisition and measurement
- Medical instrumentation

High Speed ADC Time Domain Specifications Considerations

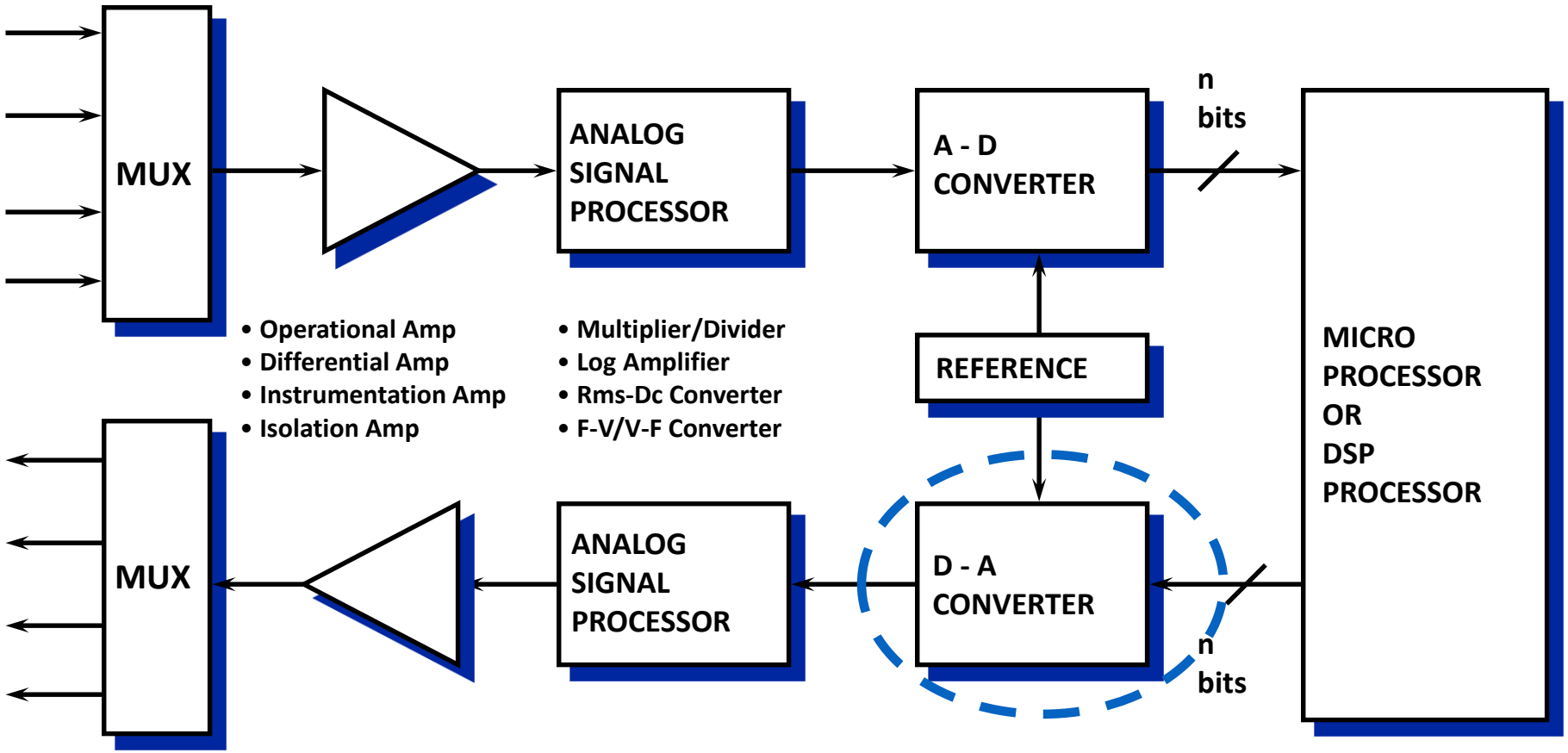
- Aperture Jitter and Delay
- ADC Pipeline Delay
- Duty Cycle Sensitivity
- DNL Effects

Animation of Analog to Digital Conversion

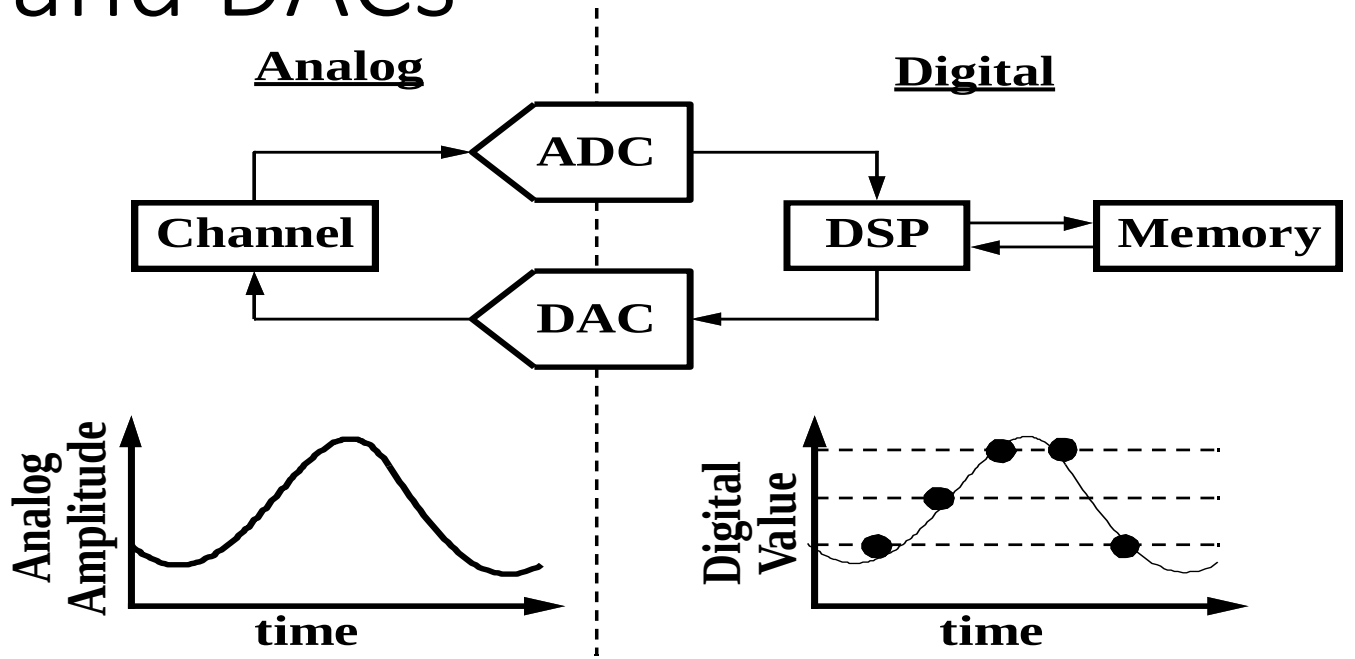
D/A Converter Introduction

- D/A Fundamentals
  - Transfer Function
  - Quantization
- Factors Affecting D/A Converter Performance
  - Static Performance
  - Dynamic Performance
- DAC Architectures
  - Resistor String
  - R-2R
  - Switched Current
- High Speed DAC Application Considerations

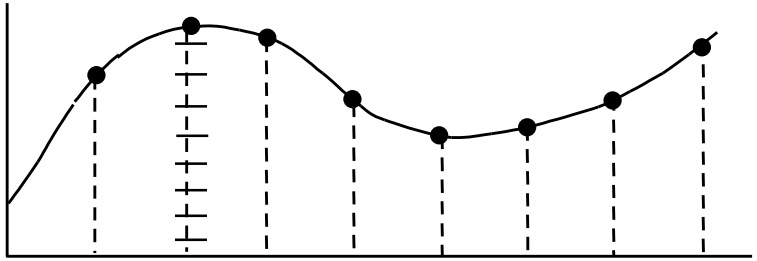
Digital to Analog Converters



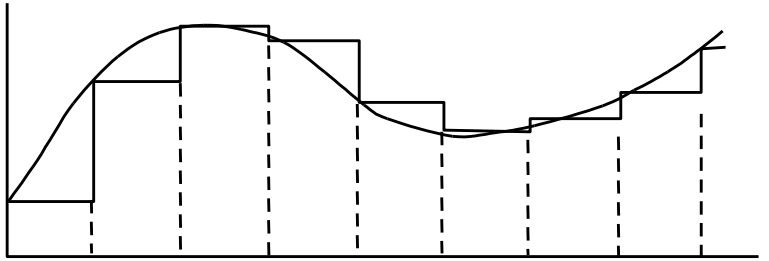
“Real World” Sampled Data Systems Consist Of ADCs and DACs



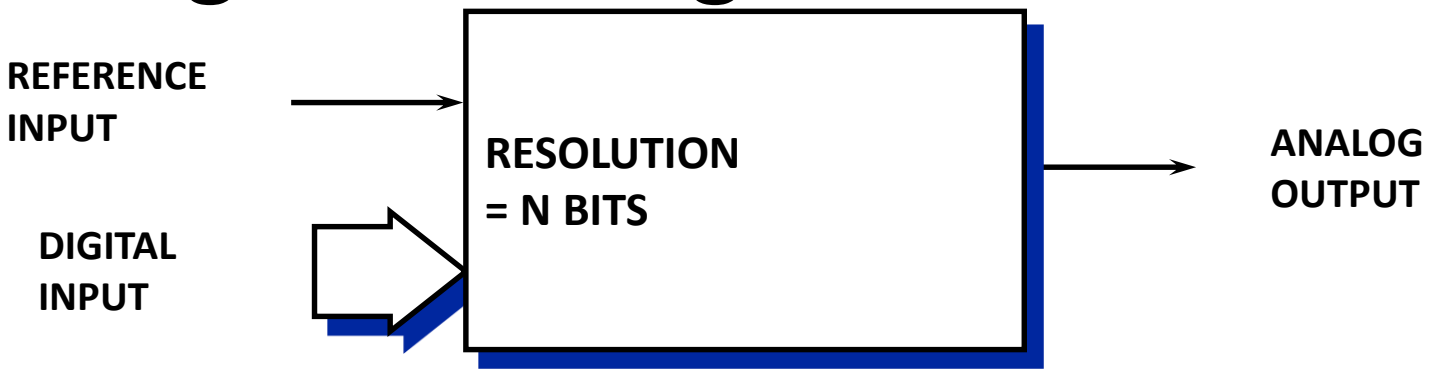
ADC SAMPLED AND QUANTIZED WAVEFORM



DAC RECONSTRUCTED WAVEFORM



What is a Digital-Analog Converter?

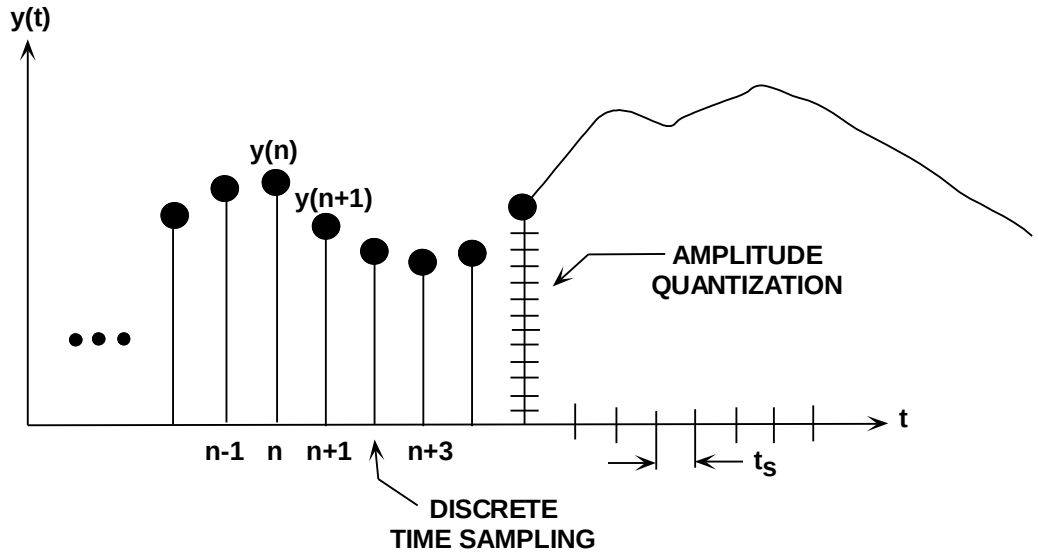


$$\text{Analog Output} = \frac{\text{Digital Input}}{(2^N - 1)} \times \text{Reference Input}$$

- Produces a Quantized (Discrete Step) Analog Output (Voltage or Current) in Response to Binary Digital Input Code
- Digital Inputs May Be TTL, ECL, CMOS, LVDS…
- A reference quantity (either voltage or current) is accurately divided into binary and/or linear segments.
- The digital input drives switches that connect an appropriate number of segments to the output.
- Finite Number of Discrete Values : 2^N Resulting in Quantization Uncertainty
- Sampling and Quantization Impose Fundamental yet Predictable Limitations

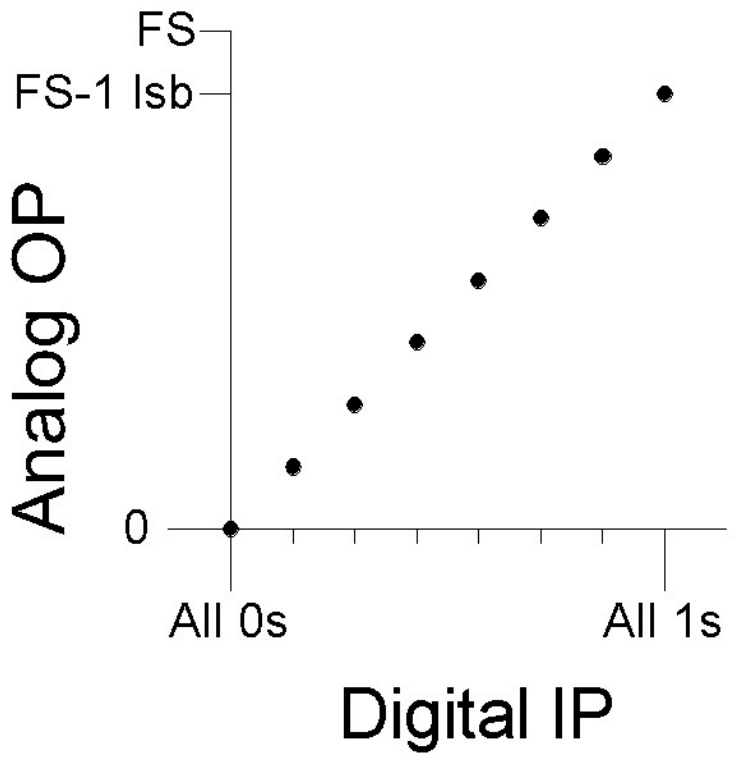
Sampling Process

- Representing a continuous time domain signal at discrete and uniform time intervals
- Determines maximum bandwidth of sampled (ADC) or reconstructed (DAC) signal (Nyquist Criteria)
- Frequency Domain- "Aliasing" for an ADC and "Images" for a DAC

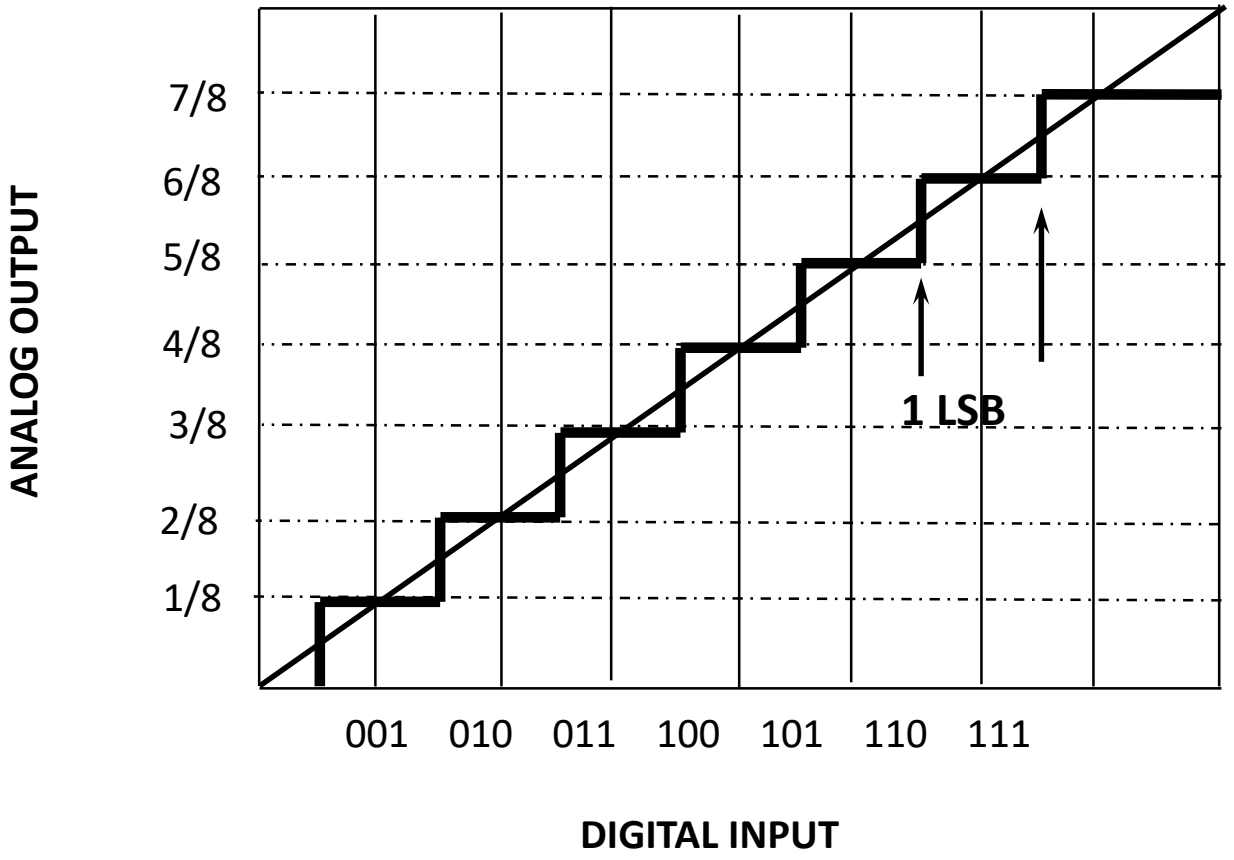


Quantization Process

- Quantization Process
  - Representing an analog signal having infinite resolution with a digital word having finite resolution and an analog output which only exists in discrete levels
  - Determines Maximum Achievable Dynamic Range
  - Results in Quantization Error/Noise



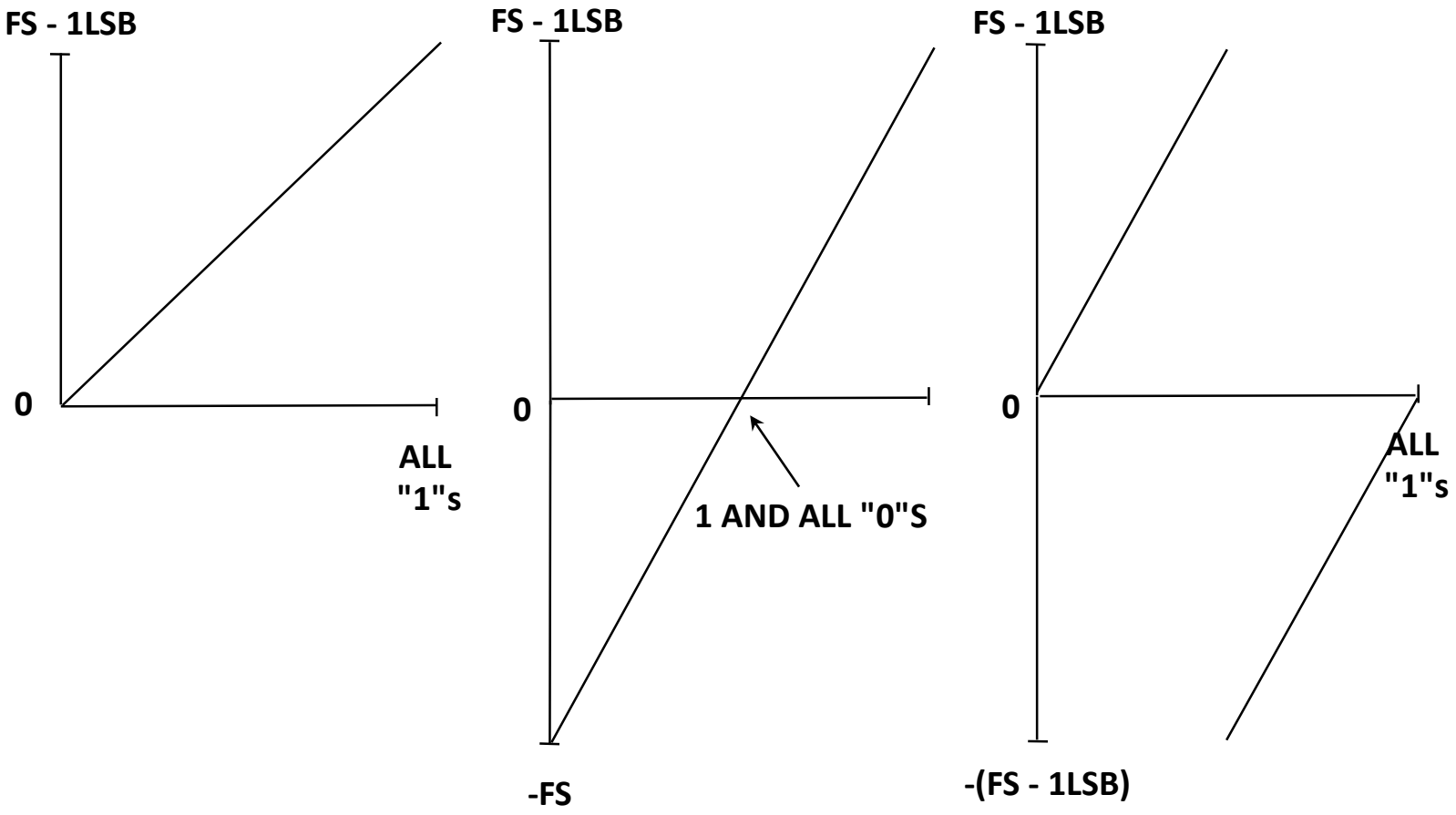
Conversion Relationship for an Ideal D/A Converter



DAC Resolution, LSBs and More...

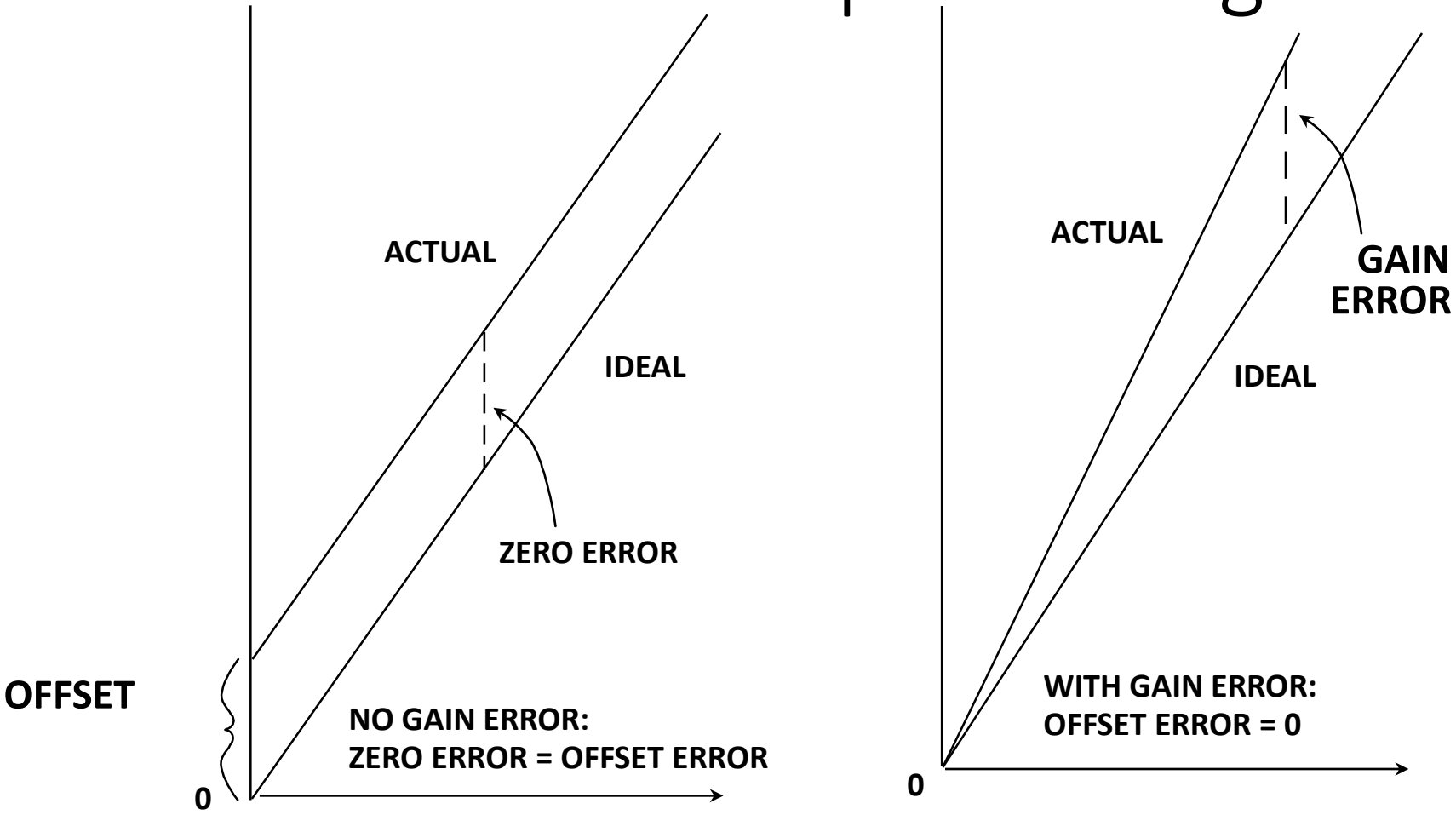
Resolution, Bits (n)	2^n	LSB, mV (10V FS)	% Full Scale	ppm Full Scale	dB Full Scale
8	256	39.1	0.391	3906	-48.0
10	1024	9.77	0.098	977	-60.0
12	4096	2.44	0.024	244	-72.0
14	16,384	0.610	0.006	61	-84.0
16	65,536	0.153	0.0015	15	-96.0
18	262,164	0.038	0.00038	3.8	-108.0
20	1,048,576	0.0095	0.00010	1.0	-120.0

Unipolar and Bipolar Converter Codes

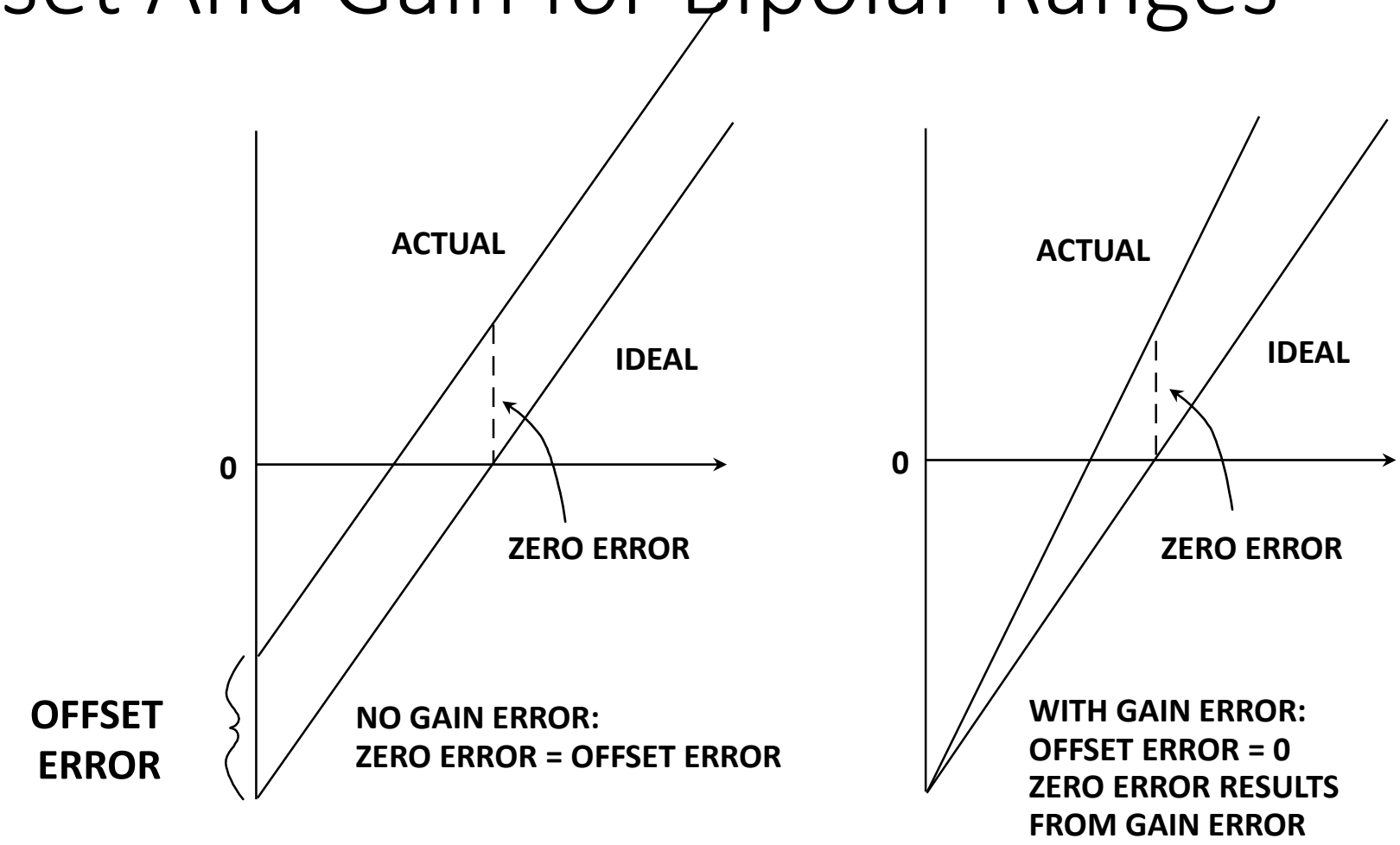


UNIPOLAR **OFFSET BINARY** **2's COMPLEMENT**

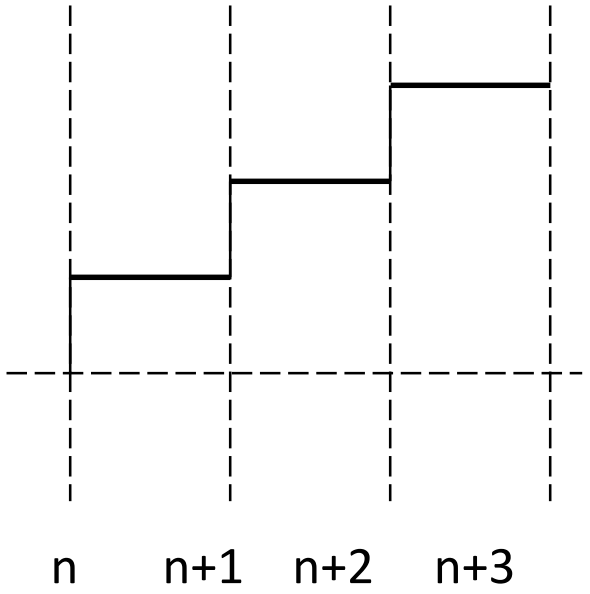
Factors Affecting D/A Converter Performance - Offset And Gain for Unipolar Ranges

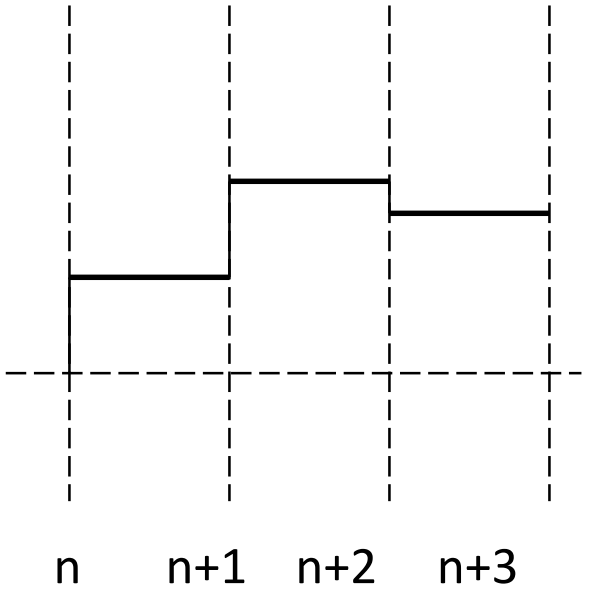


Factors Affecting D/A Converter Performance - Offset And Gain for Bipolar Ranges

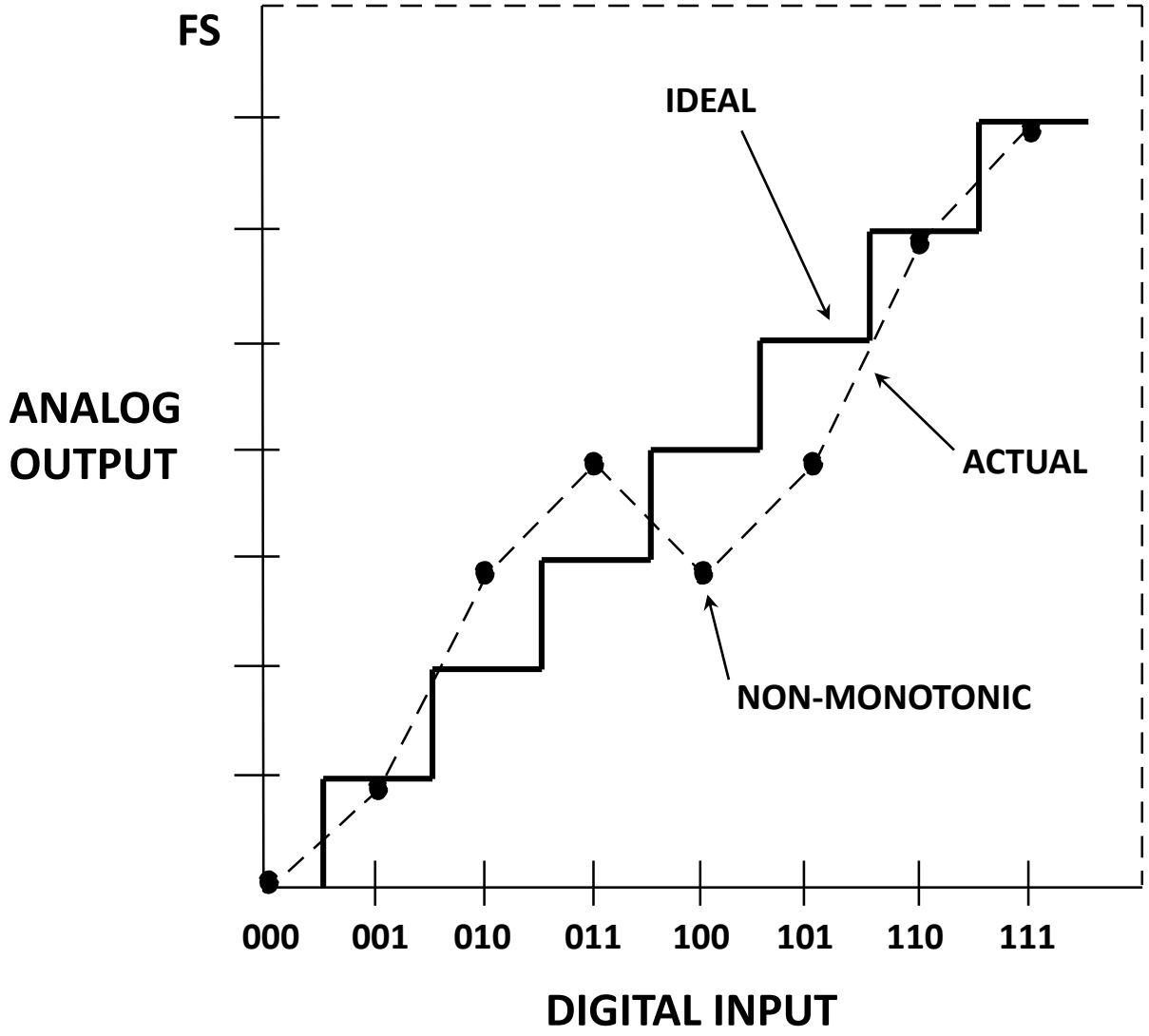


Monotonicity

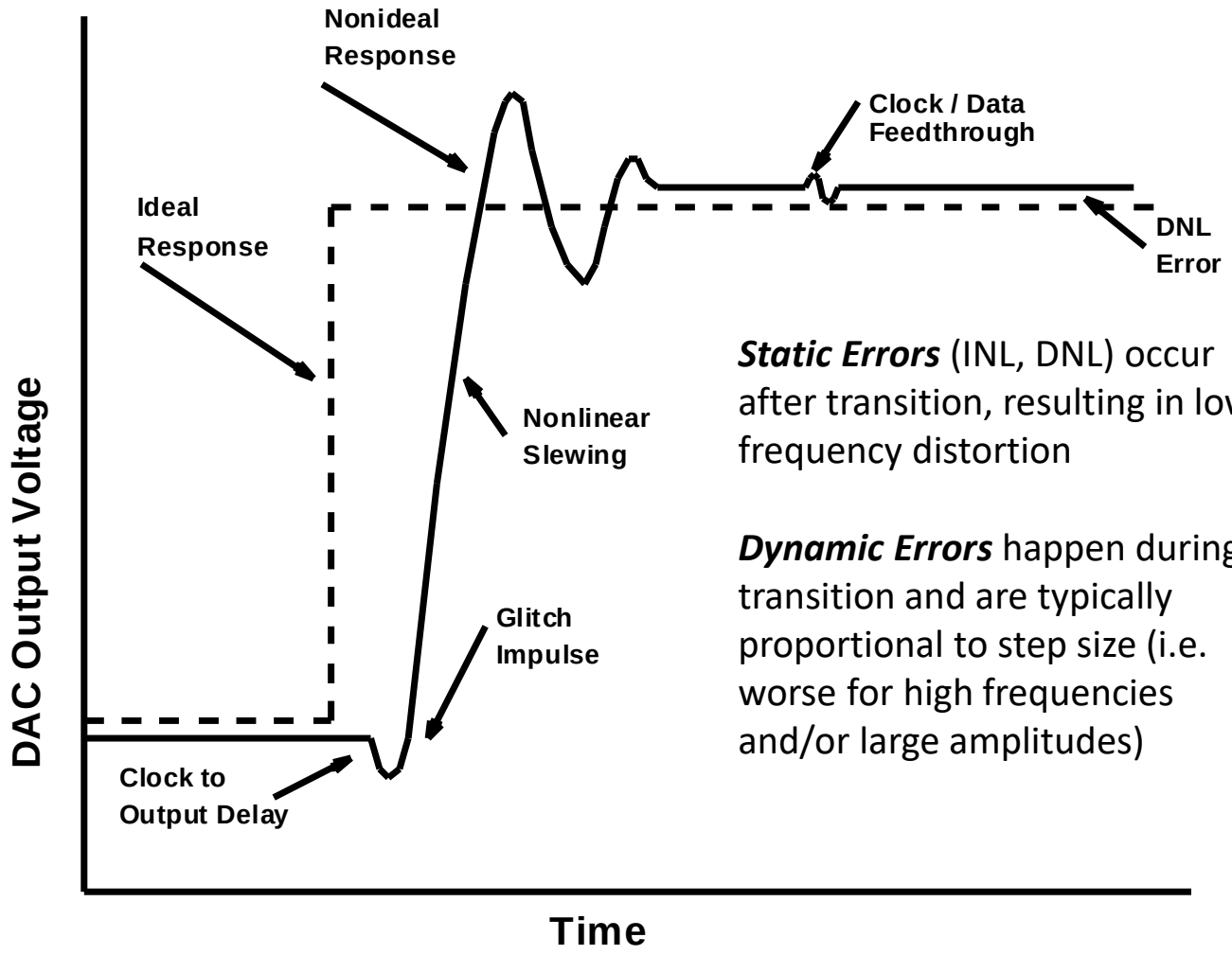




Monotonicity



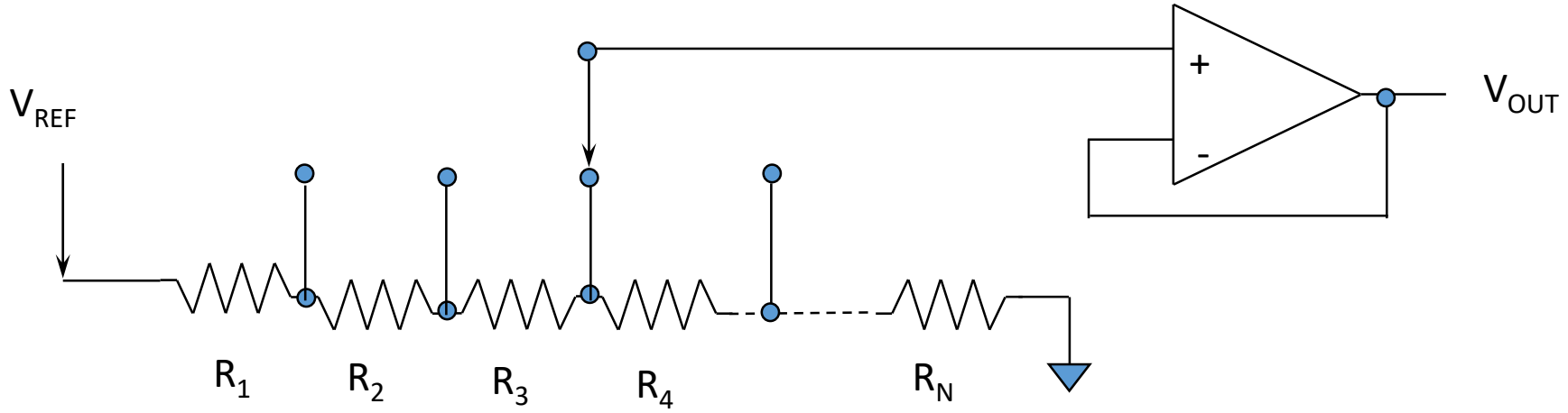
Settling Issues



Static Errors (INL, DNL) occur after transition, resulting in low-frequency distortion

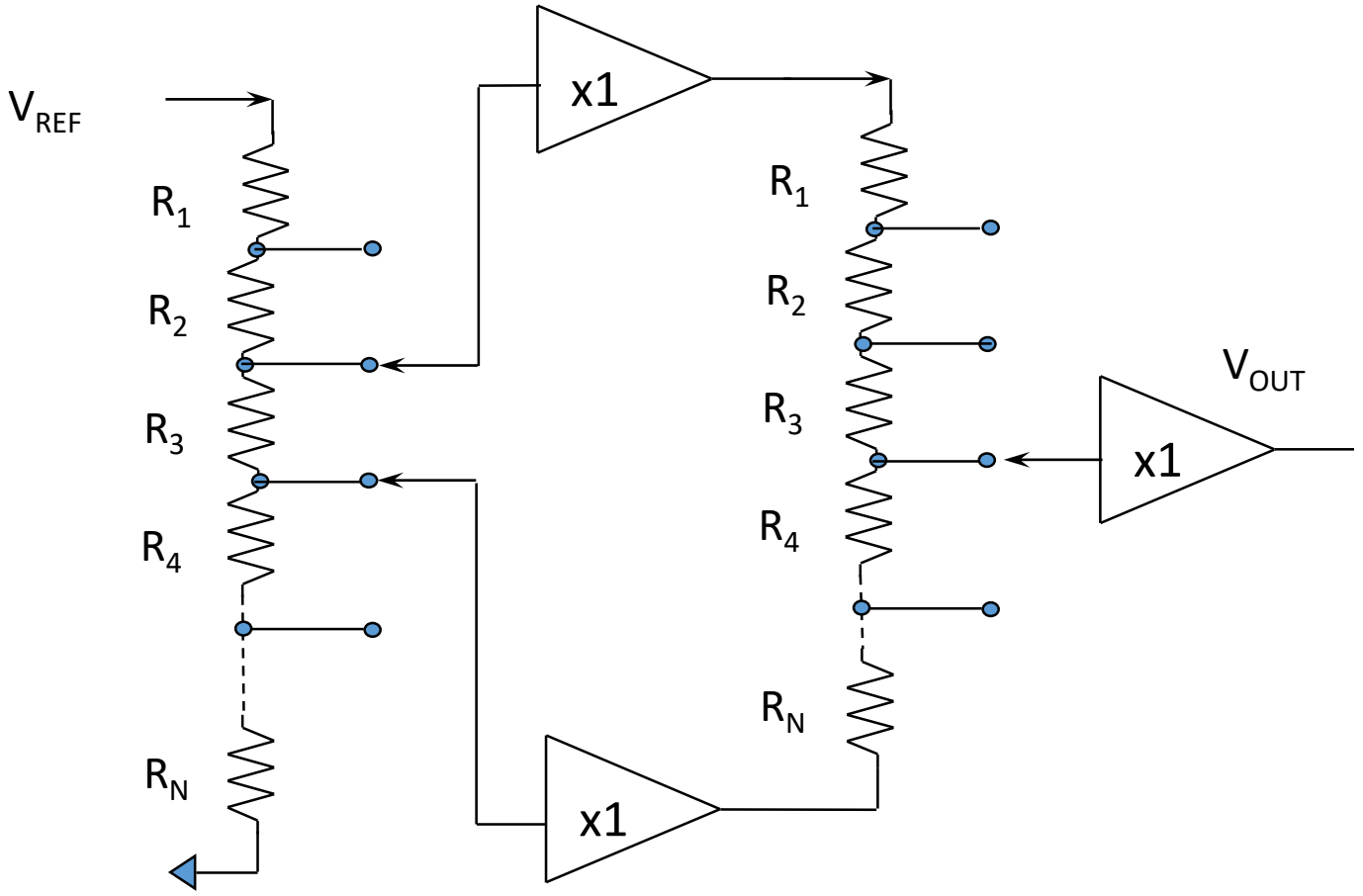
Dynamic Errors happen during transition and are typically proportional to step size (i.e. worse for high frequencies and/or large amplitudes)

A Simple D-A Converter Using a Kelvin Divider

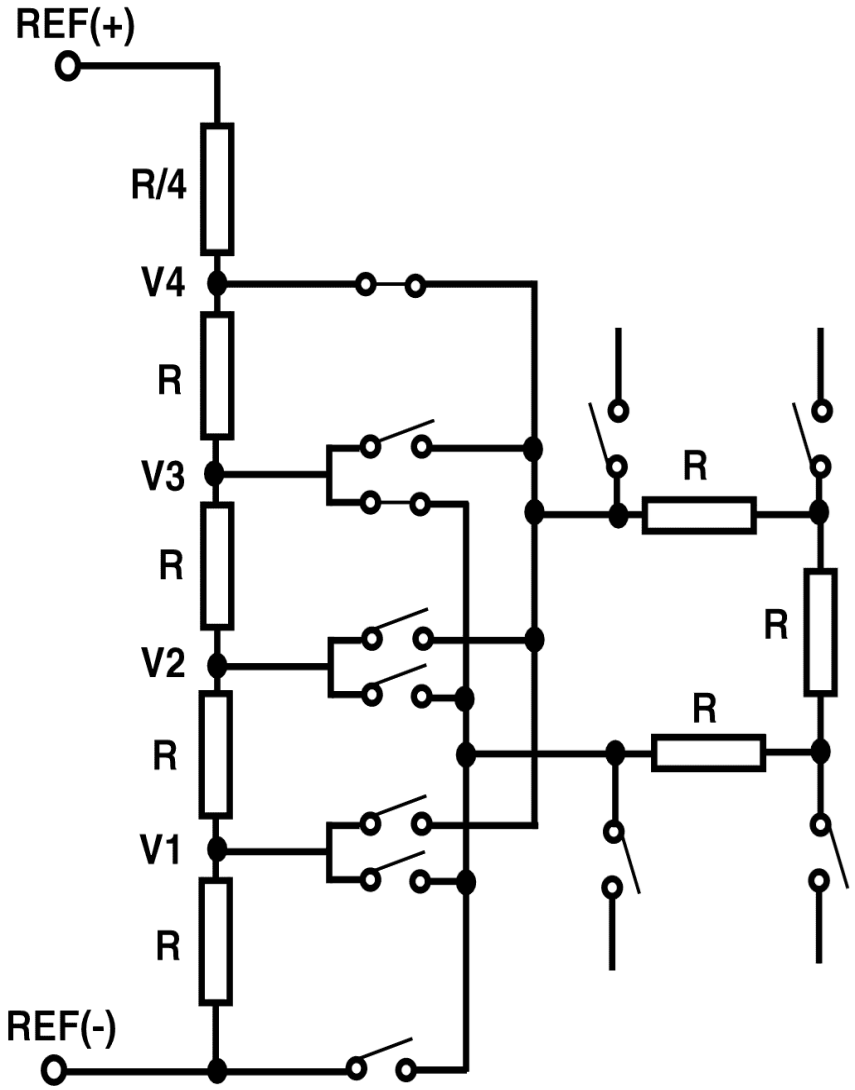


- Not a Practical Approach
- Output is Monotonic
- For N Bit Resolution, 2N Resistors (Taps) are Required

Voltage Segment DAC

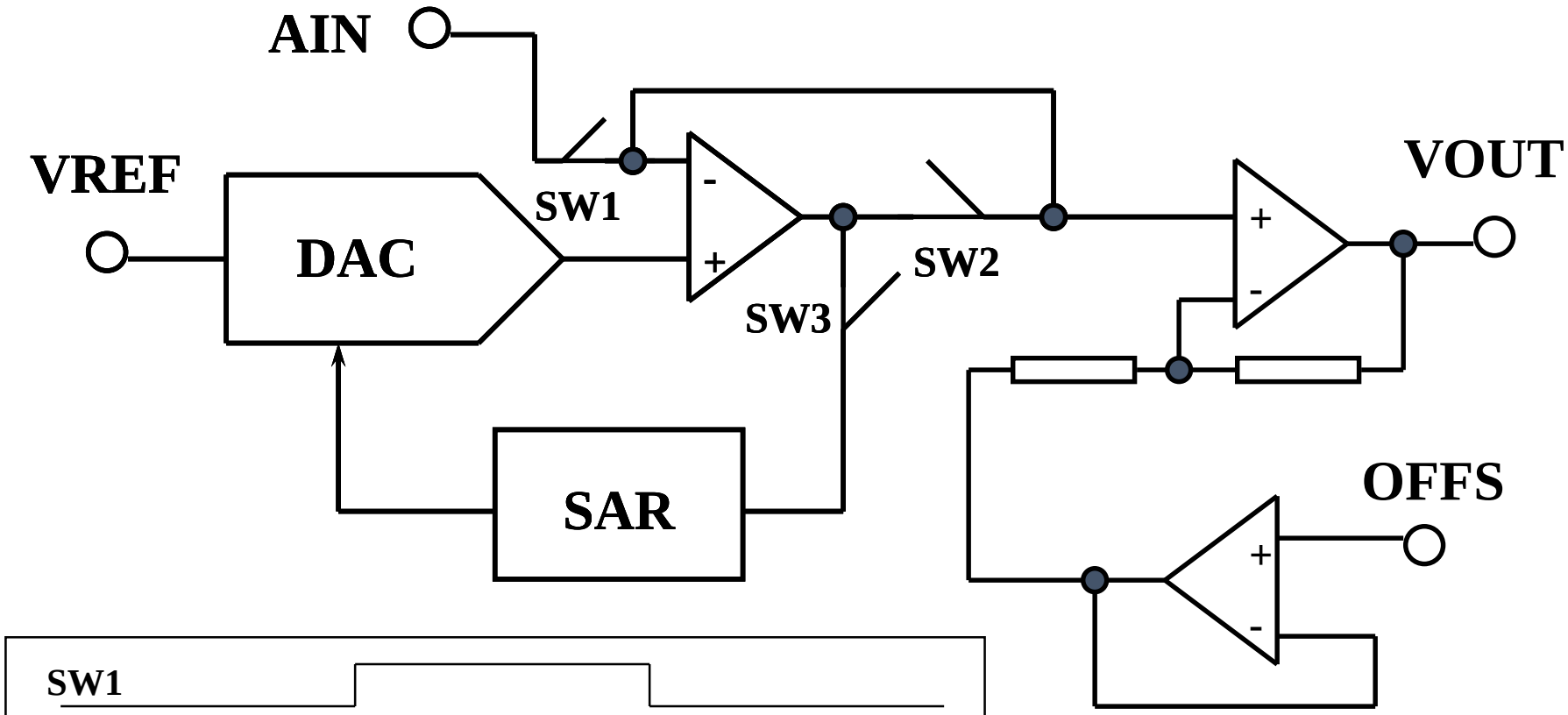


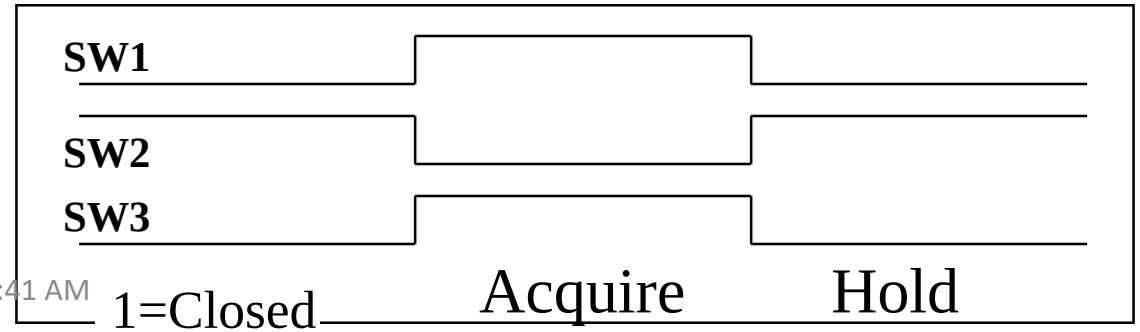
STRING DAC Architecture



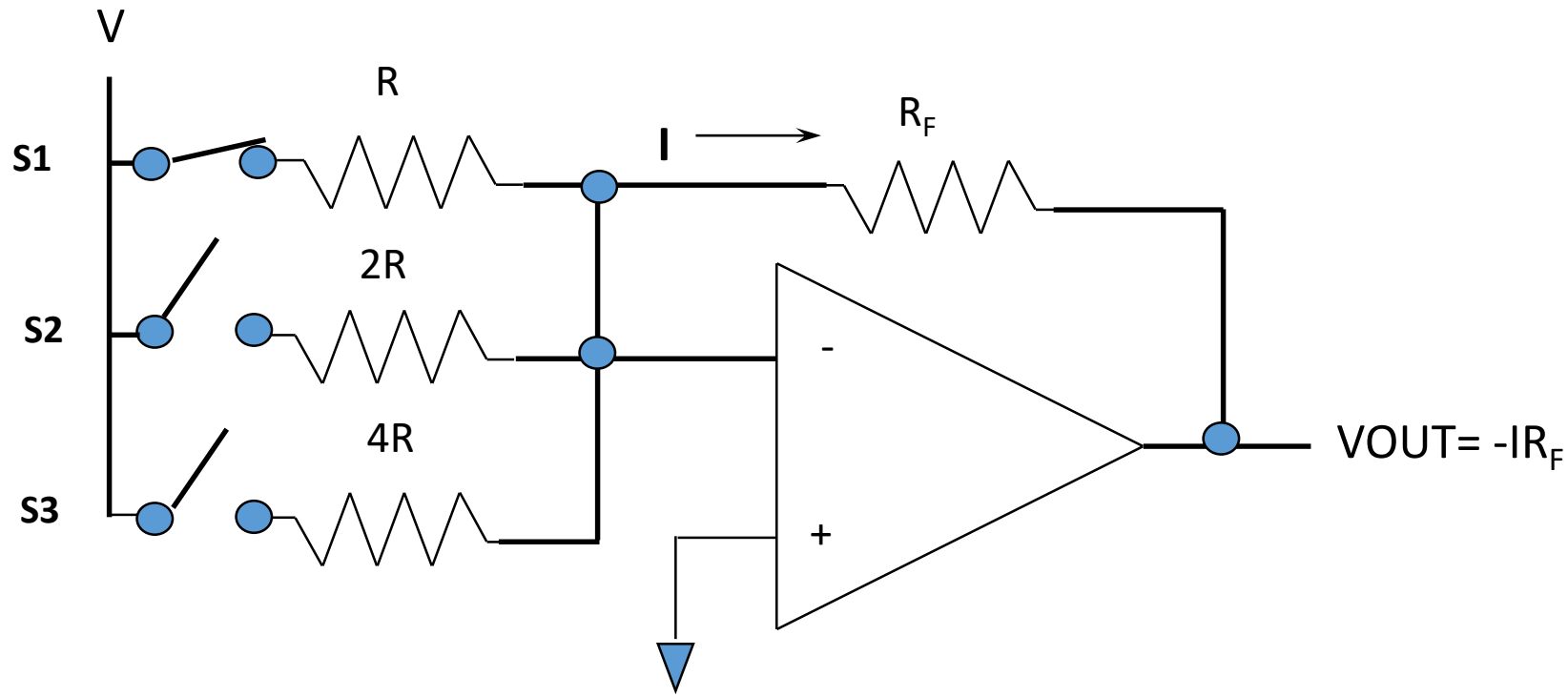
- Traditional String DAC requires 2^n Resistors.
- Main DAC and Sub-DAC leads to $2^{N/2} + (2^{N/2} -1)$ Resistors
- Vsubdac=Rll(3R)=3R/4. VREF=1
- Rtotal=R/4+(3R)/4+3R = 4R
- LSB = Vsubdac/3=R/4
- Size, Power, and Cost Reduction.
- Resistor Matching Excellent- DPDM, no Trimming.
- Guaranteed Monotonic
- Voltage Output

Infinite Sample and Hold Architecture



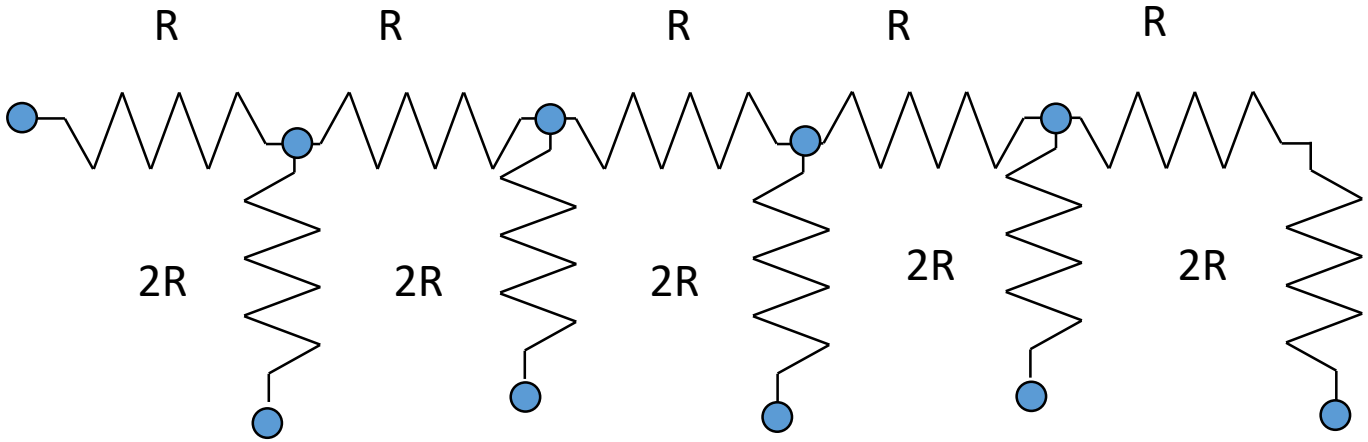


A Simple Binary-Weighted D-A Converter



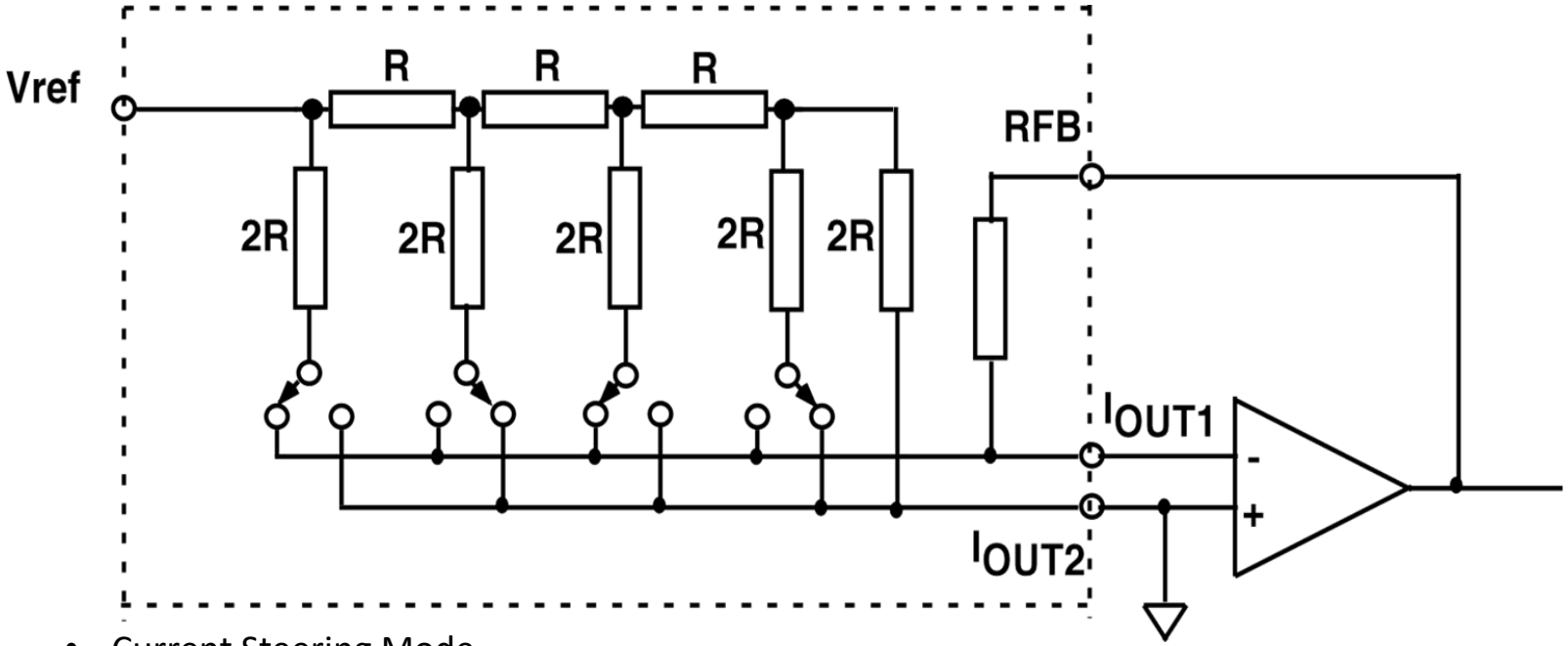
- A Simple Binary-Weighted Network. The Current I is the Sum of the Individual Currents Through R, 2R and 4R.

R-2R Ladder Network



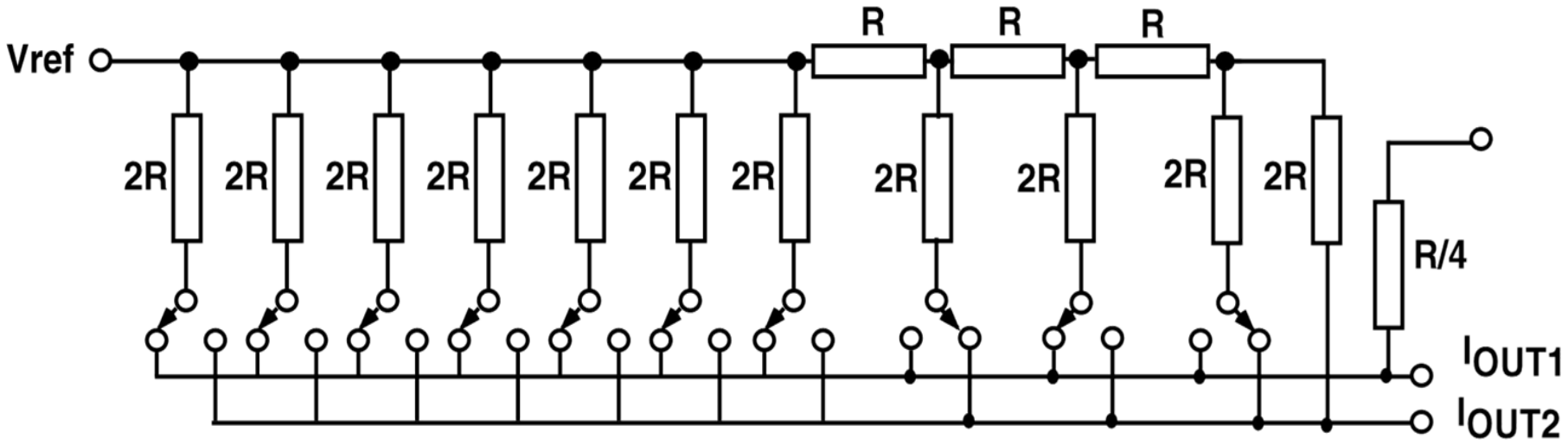
- R and 2R Values Easy to Trim in Production
- Match to 1 Part in 2n Will Yield n Monotonicity
- Absolute Value Not Important (typ. 10-20 kΩ, +/-20%)
- Voltage vs. Current Switching Mode

Current Steering Mode



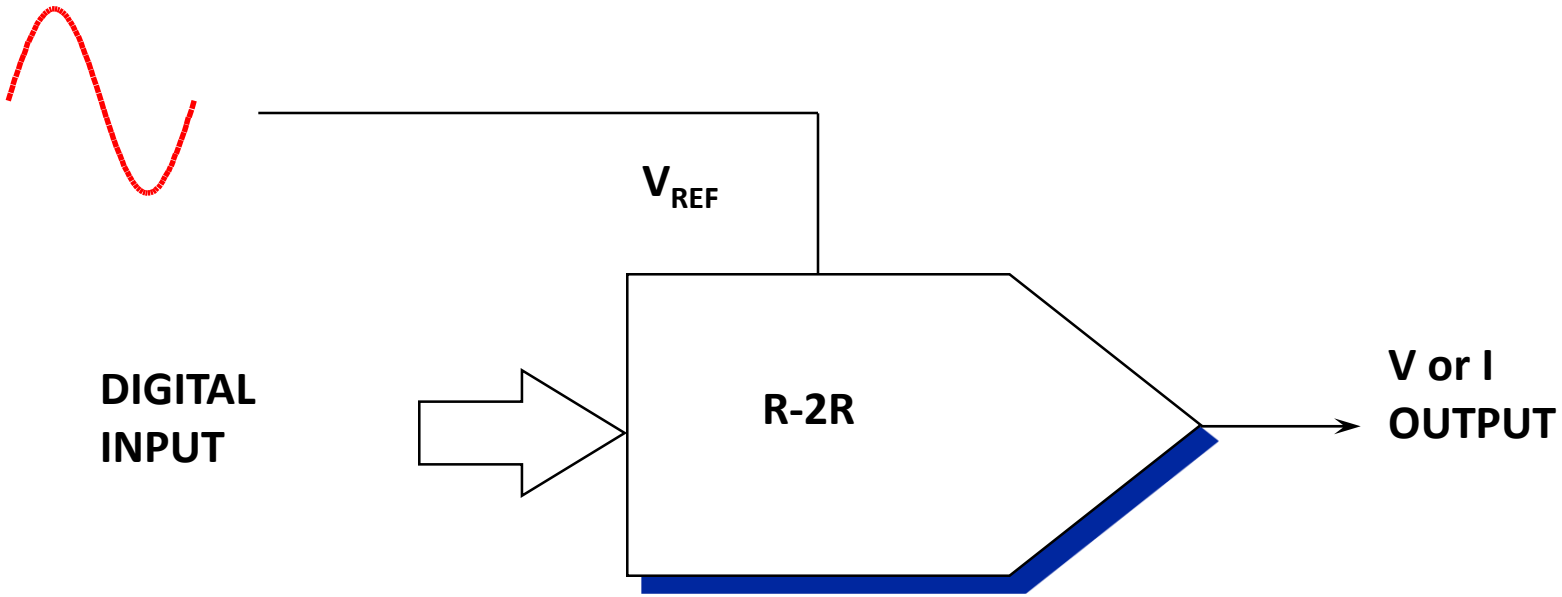
- Current Steering Mode
- Constant Input Impedance
- Output Impedance Varies with Code
- Vout = -D X V_{ref}
- REF Bandwidths < 1 MHz
- Nonlinearity Increases with Decreasing Reference

Segmented R-2R

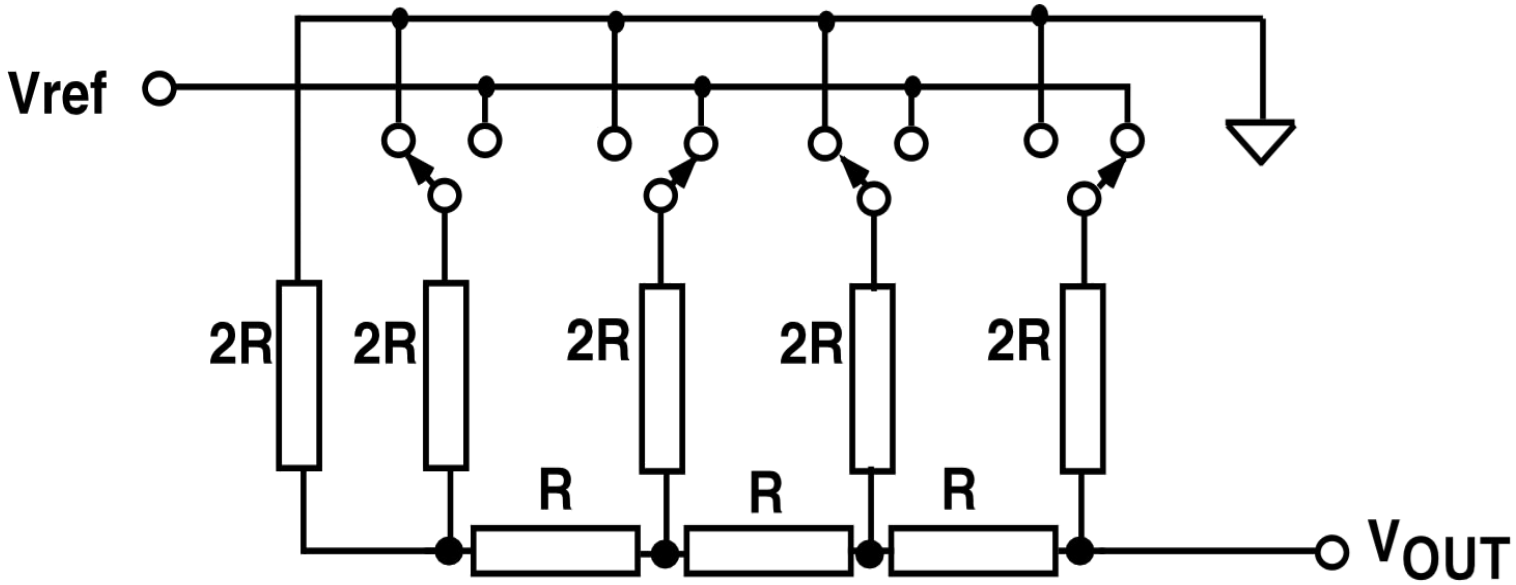


- 3, 4 or 5 Fully Decoded MSBs followed by R2R Ladder for LSBs
- Less Trimming in Production for Higher Resolution DACs
- Linearity Specs more readily achievable
- Lower Input Impedance - Less Distortion.
- Fixed Input Impedance.

“Multiplying” DAC

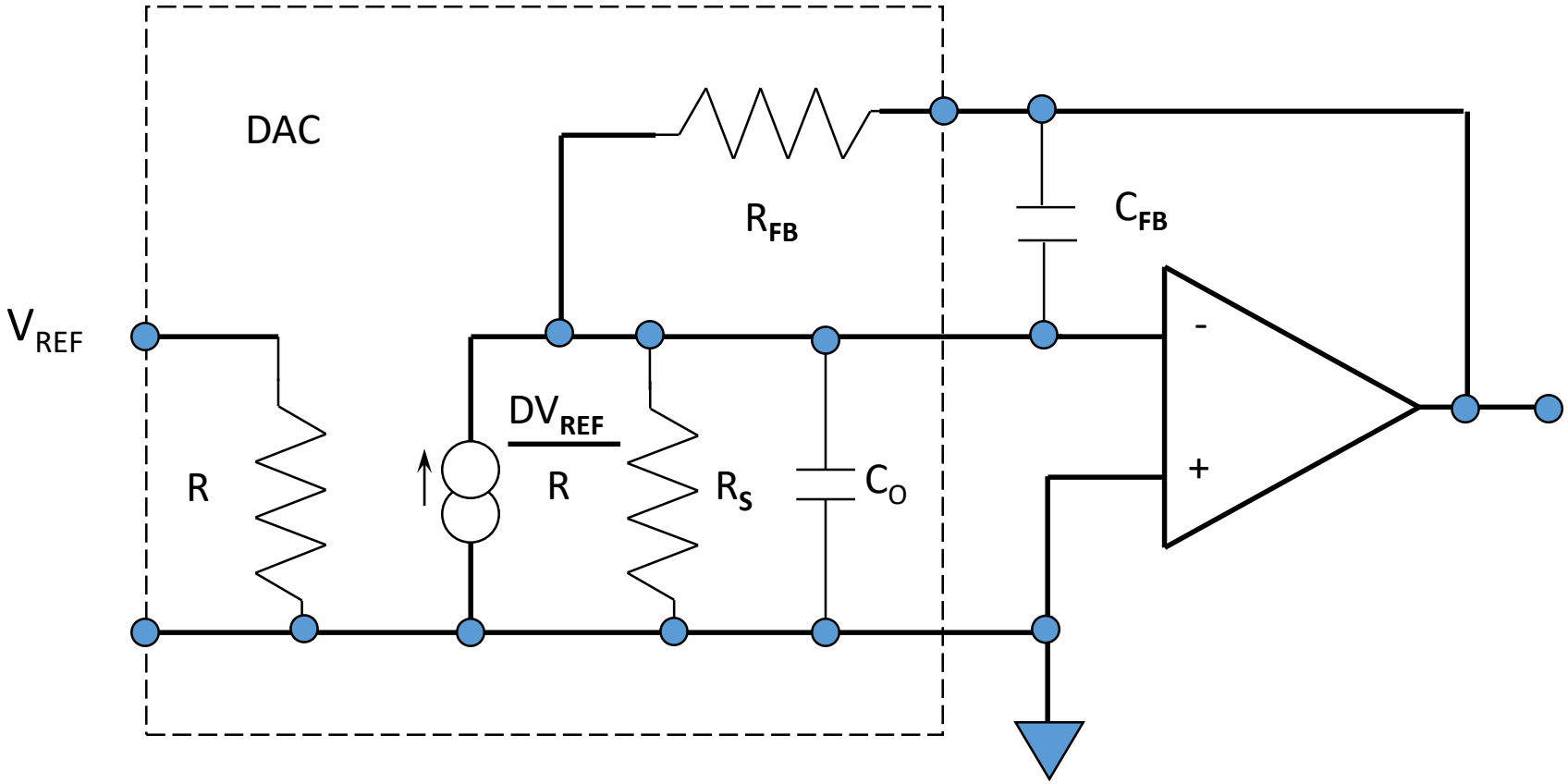


Voltage Switching Mode



- Output Voltage is Same Polarity as Input
- Constant Output Impedance
- Input Impedance Varies With Code
- V_{REF} Limited to 2.0-2.5 Volts
- Allows Single Supply Operation

CMOS R-2R DAC Equivalent Circuit

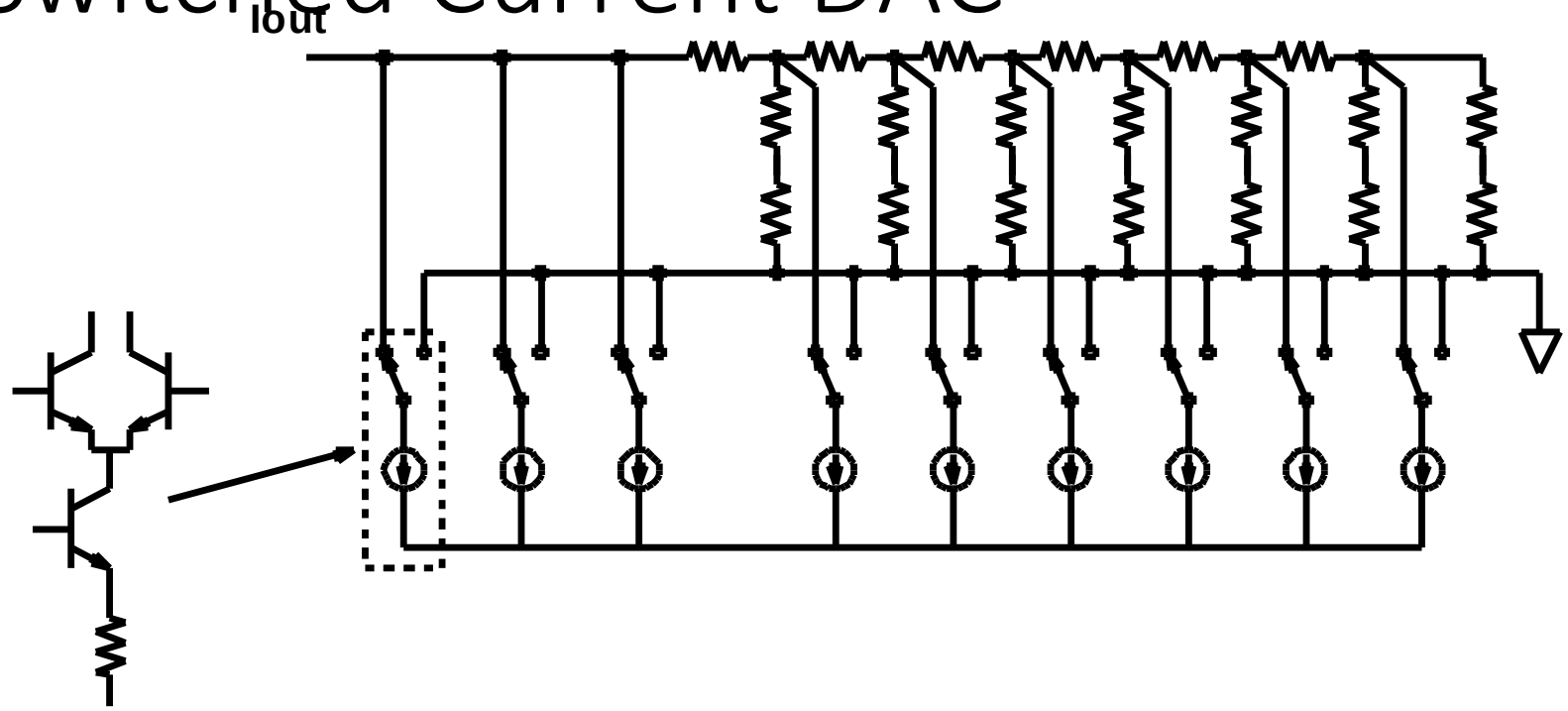


CMOS DAC Equivalent Circuit (con’t)

- R is the Ladder Resistance Seen By The Reference (typ 10-20 kilohms).
- VREF/R = Full Scale Current Output
- D = Digital Code Ratio
- RO, CO = Code-Dependent Output Resistance and Capacitance
- RFB = DAC Internal Feedback Resistor For Use With External Amplifier. Matched and Tracking With R-2R Ladder.
- CFB = Compensation Capacitance for CO.

$$= \sqrt{\frac{C_O}{2 \times \pi \times BW}}$$ **; BW = Unity Gain Bandwidth**

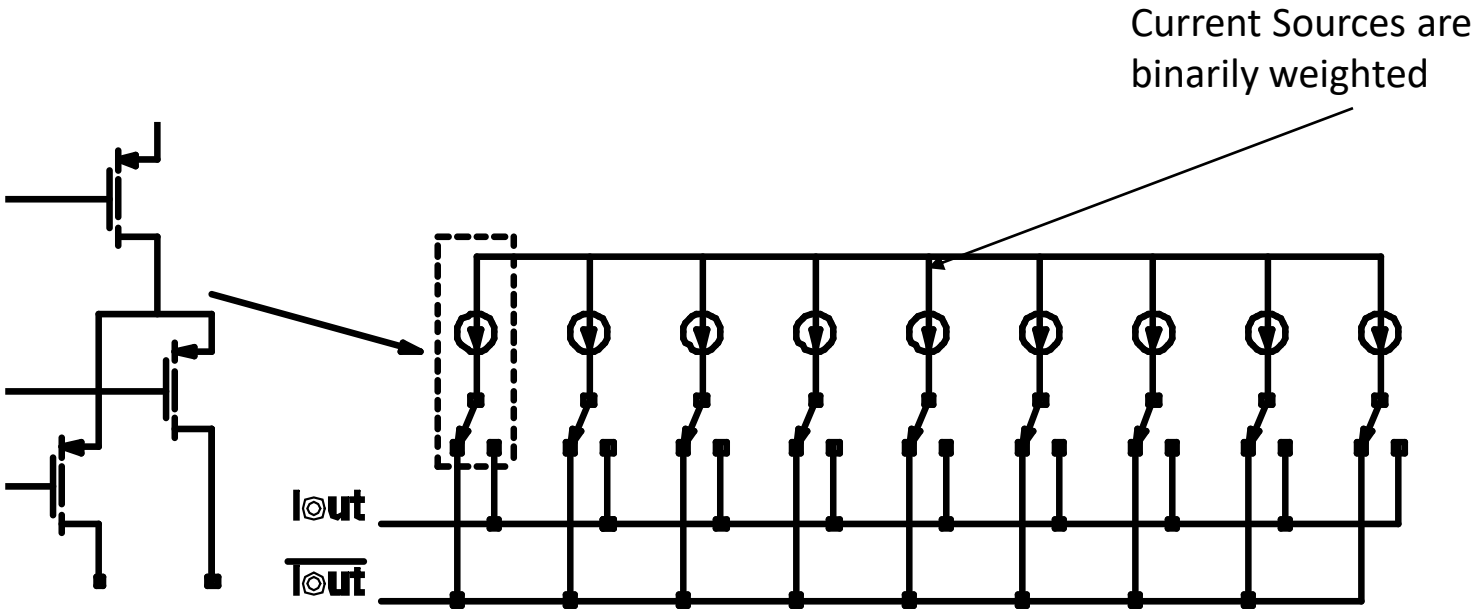
Bipolar Switched Current DAC



- Good device matching results in good DC performance
- Device scaling difficult, requires R-2R for higher resolution
- Typically higher power, can’t integrate Digital Signal Processing

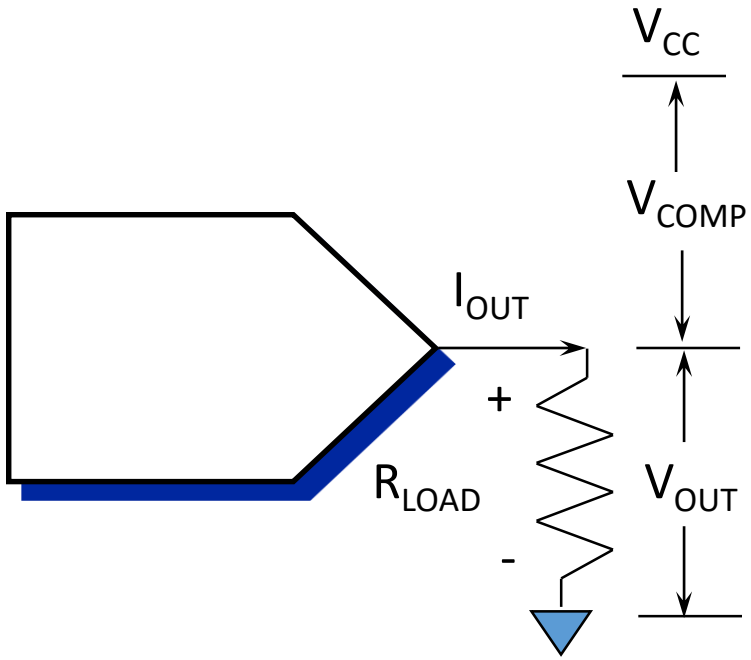
CMOS Switched Current DAC

- Scaling issues are simplified, no need for R-2R
- Allows Integration of Digital Signal Processing
- Good Device Matching for 12-bit linearity, calibration required for higher resolution
- Popular in Communications applications



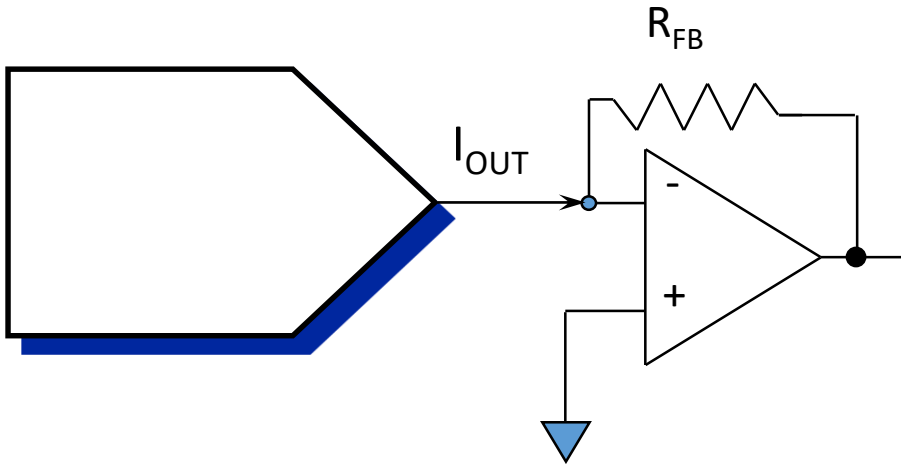
Terminating a Current Output DAC

Best AC performance



Compliance Voltage

Best DC Performance



Virtual Ground

Architecture Pros and Cons

- Summary:
  - Resistor String
    - Inherent Monotonicity
    - Compact Design Leading to the basis of Multi-Channel DACs
    - Difficult to get High performance INL
  - R-2R Ladder
    - Good DC performance
    - Suffer from distributed R-C effects and signal-dependant loading in frequency-domain applications
    - Multiplying Capability
    - Can Operate in Voltage Mode for Single Supply Applications

Architecture Pros and Cons

- Summary (con’t):
  - Bipolar Switched Current
    - Suffers AC limitations because R-2R is typically required to create LSB currents
  - CMOS Switched Current
    - Best Choice for frequency-domain applications:
      - No R-2R to limit AC performance
      - Good matching for DC specifications (calibration sometimes needed)
      - Allows for integration with discrete signal processing blocks to ease implementation and improve performance